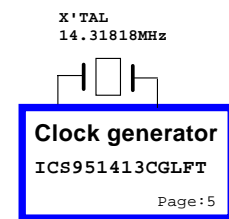
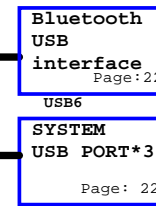
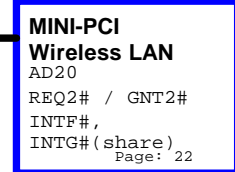
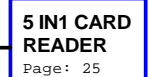
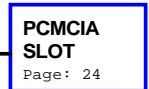
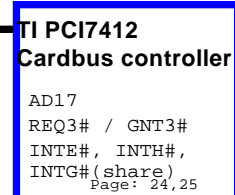
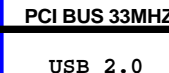
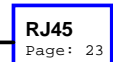
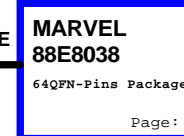
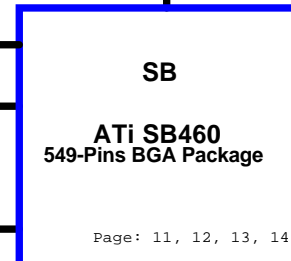
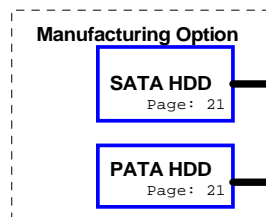
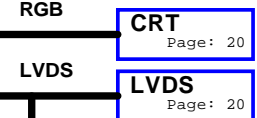
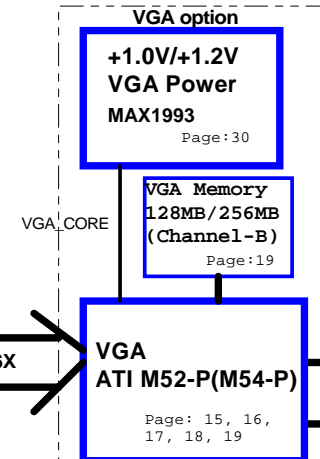
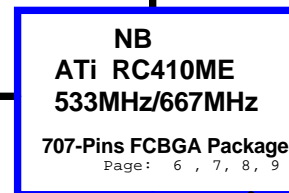
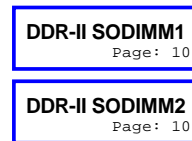
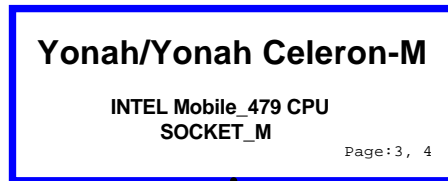


Power State Table

Power Name	Control Signal	Power State
VCC_CORE	VRON	S0
VCCP_+1.05V	MAINON	S0
+3VPCU	N/A	ALWAYS
+3V_S5	S5_ON	S0-S5
+3VSUS	SUSD	S0-S3
+3V	MAIND	S0
+5VPCU	N/A	ALWAYS
+5VSUS	SUSD	S0-S3
+5V	MAIND	S0
15V	N/A	S0
+1.2V	MAINON	S0
VGA_CORE	VGA_MAINON	S0
+2.5V	MAINON (Delay 1ms)	S0
+0.9V_VTER	MAINON	S0
+1.8V_S5	S5_ON	S0-S5
+1.8VSUS	SUSON	S0-S3
+1.8V	MAIND	S0
+1.5V_RUN	MAINON	S0



## ZB3



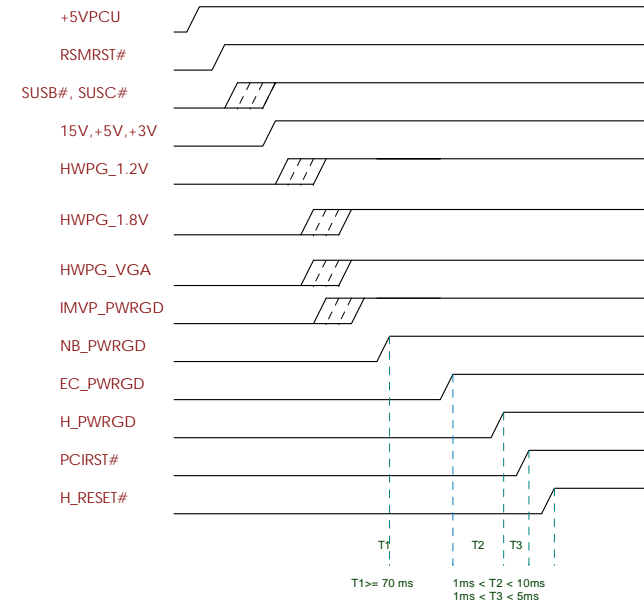
# TABLE OF CONTENTS

Page 01 : BLOCK DIAGRAM  
Page 02 : TABLE OF CONTENTS  
Page 03 : Yanah CPU(HOST Bus)-1  
Page 04 : Yanah CPU(POWER/NC)-2  
Page 05 : CLOCK GENERATOR  
Page 06 : RC410ME-MEMORY\_AGTL+ I/F  
Page 07 : RC410ME-PCIE LINK EXTERNAL VGA  
Page 08 : RC410ME-LVDS OUT & CLKGEN  
Page 09 : RC410ME-POWER  
Page 10 : DDR2 SO-DIMM X2 & TERMINA  
Page 11 : SB460M-PCIE/PCI/CPU/LPC  
Page 12 : SB460M ACPI/GPIO/USB/AC97  
Page 13 : SB460M HDD/POWER/DECOUPLI  
Page 14 : SB460M STRAPS  
Page 15 : M52-P\_MAIN\_PCIE (1 of 4)  
Page 16 : M52-P\_MEM\_GND (2 of 4)  
Page 17 : M52-P\_Power\_LVDS(3 of 4)  
Page 18 : M52-P\_Straps (4 of 4)  
Page 19 : VGA RAM (64BIT DDR2)  
Page 20 : CRT & LVDS  
Page 21 : HDD & CDROM ,HOLES  
Page 22 : MINI PCI, USB Bluetooth PORT  
Page 23 : LAN PCI-E EE88038  
Page 24 : PCI7412-PCMCIA CONTROLLE  
Page 25 : PCI7412-CARD READER  
Page 26 : CODEC T/P MIC/LINE-IN/OUT-ALC883  
Page 27 : AUDIO AMP&LINE OUT  
Page 28 : PC97551 & FLASH  
Page 29 : FAN,SWITCH,LED,KB  
Page 30 : VGA CORE 1.0V/1.2V  
Page 31 : CPU CORE-MAX8736ETL+  
Page 32 : +VCCP(1.05V)& 1.2V(NB PWR  
Page 33 : DDRII PWR\_1.8VSUS-VTERM  
Page 34 : SYSTEM +5V& +3V MAX1999A  
Page 35 : BATTERY CHARGER

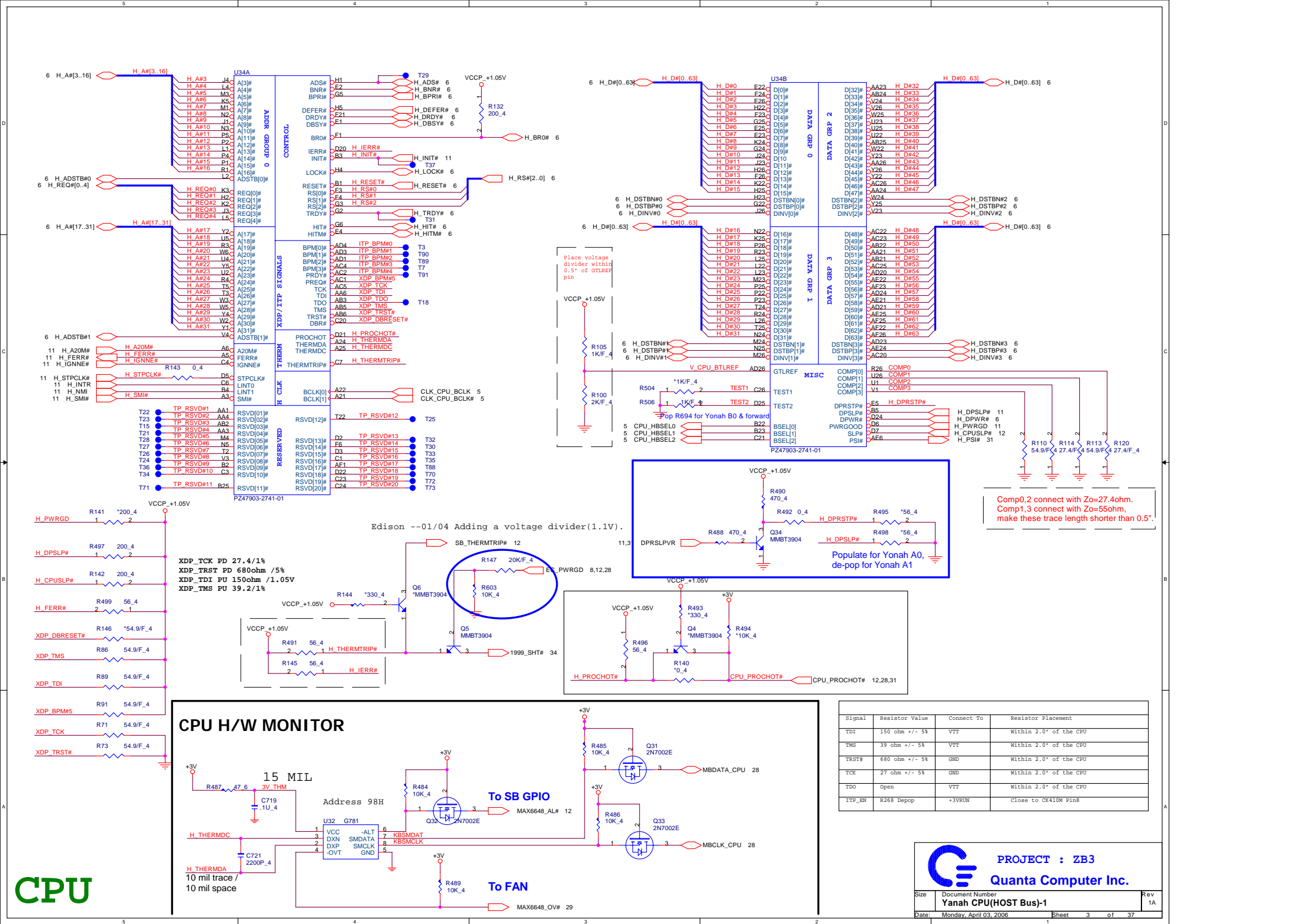
## POWER VOLTAGE ACTIVE SCOPE PAGE

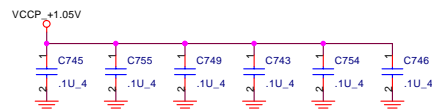
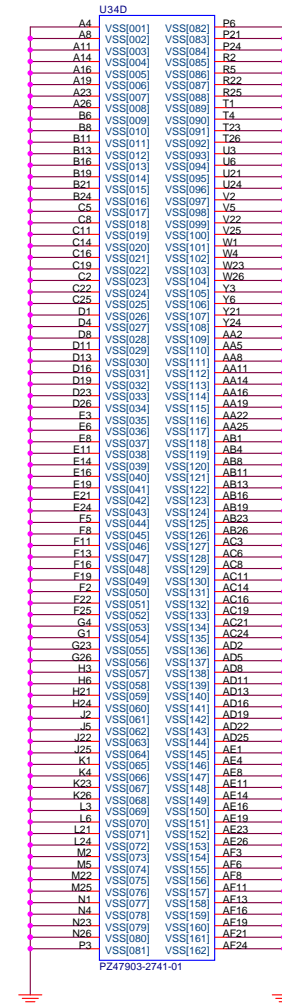
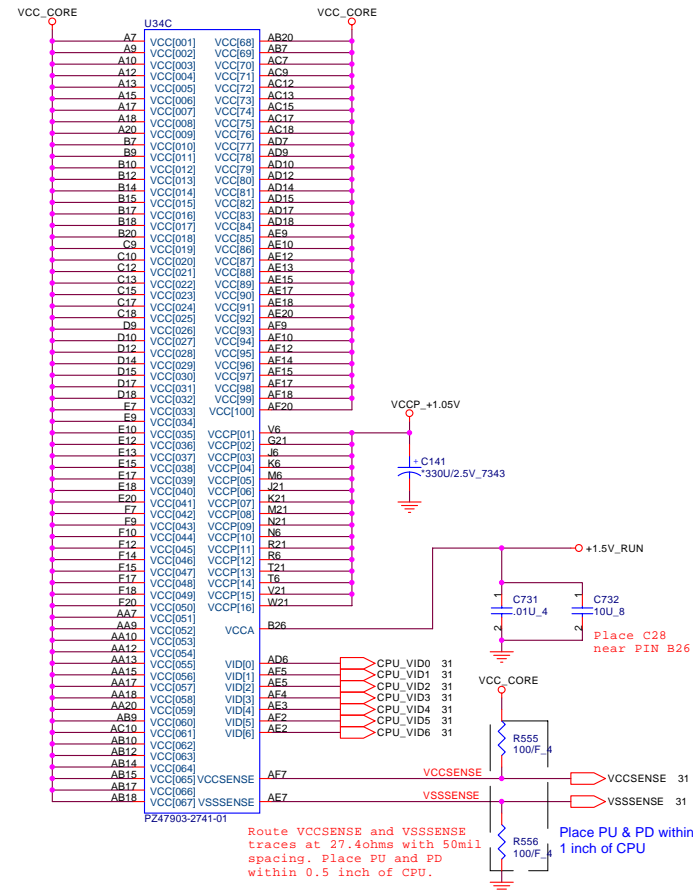
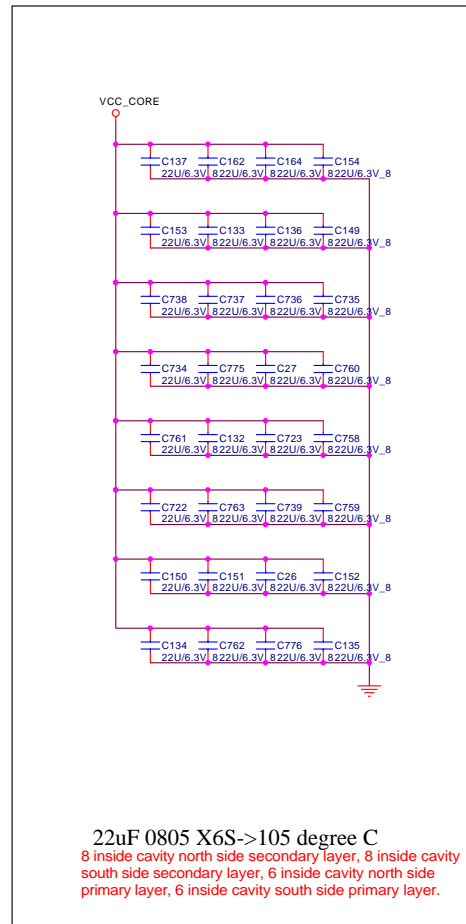
SYSTEM	15V	15V	S0	33
	+5V	+5V	S0	33
	+3V	+3.3V	S0	33
	+5VPCU	+5V	ALWAYS	33
	+3VPCU	+3.3V	ALWAYS	33
	+5VSUS	+5V	S0-S3	33
	+3VSUS	+3.3V	S0-S3	33
CPU	+3V_S5	+3.3V	S0-S5	33
	VCC_CORE	VID[0..6]	S0	31
	VCCP_+1.05V	+1.05V	S0	31
RC410ME NB	+1.5V_RUN	+1.5V	S0	31
	VCCP_+1.05V	+1.05V	S0	31
	+1.8V	+1.8V	S0	33
	+1.8VSUS	+1.8V	S0-S3	33
	+1.2V	+1.2V	S0	32
	+3V	+3.3V	S0	33
	+1.2V_PCIE	+1.2V	S0	9
	+1.2V_CORE	+1.2V	S0	9
	VDD18	+1.8V	S0	9
	VDDA18	+1.8V	S0	9
	NB_VDDR	+3.3V	S0	8
	AVDD_NB	+3.3V	S0	8
	AVDDQ	+1.8V	S0	8
	PLVDD	+1.8V	S0	8
	NB_LPVD	+1.8V	S0	8
	NB_LVDDR18A	+1.8V	S0	8
SB460 SB	+3V	+3.3V	S0	33
	+1.8V	+1.8V	S0	33
	+3V_S5	+3.3V	S0-S5	33
	+1.8V_S5	+1.8V	S0-S5	30
	VCCP_+1.05V	+1.05V	S0	31
	+1.8VUSB_PHY	+1.8V	S0-S5	13
	V5_REF	+5V	S0	13
	+1.8V_ATA	+1.8V	Reserve	13
	PLLVD_ATA	+1.8V	Reserve	13
	XTLVDD_ATA	+1.8V	Reserve	13
	PCIE_PVDD	+1.8V	S0	11
	PCIE_VDDR	+1.8V	S0	11
	AVDD_USB	+3VSUS	S0-S3	12
	+3.3V_AVDDC	+3.3V	S0-S3	12
	VCCRTC	+3.0V	--	11
	VDDQ_3V	+3.3V	S0	13
	VDD_1.8V	+1.8V	S0	13
	SB_S5_3V	+3.3V	S0-S5	13
	SB_S5_1.8V	+1.8V	S0-S5	13
	AVDD_CK_1.8V	+1.8V	S0	13
DDR2	+1.8V	+1.8V	S0	33
	+1.8VSUS	+1.8V	S0-S3	10
	+0.9V_VTER	+0.9V	S0	10

## POWER UP SEQUENCE



PROJECT : ZB3  
Quanta Computer Inc.





CPU

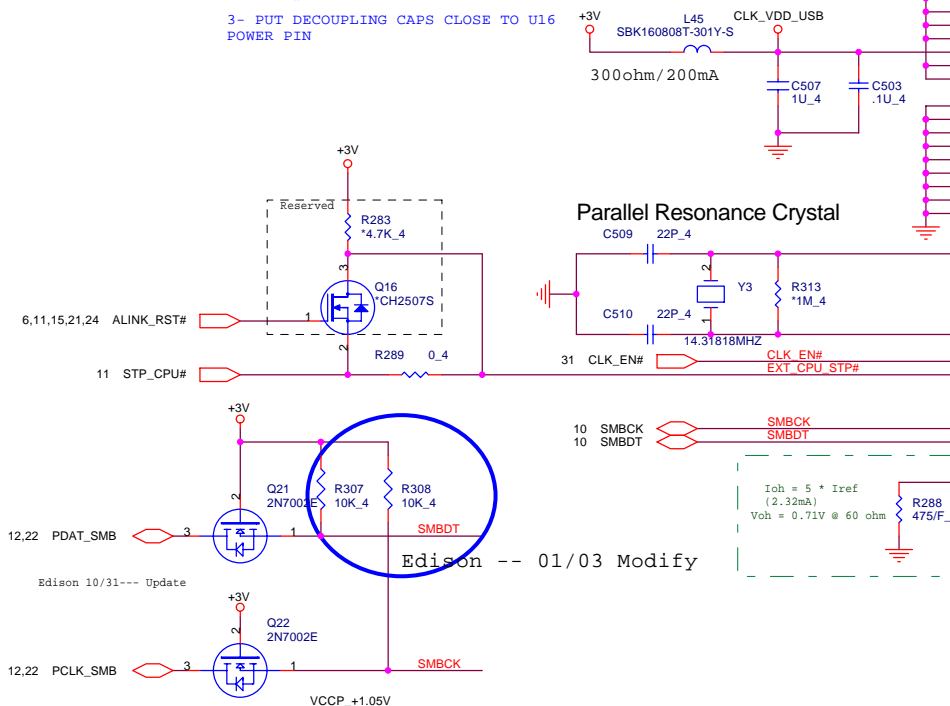
```

1- PLACE ALL THE SERIES TERMINATION
RESISTORS AS CLOSE AS U16 AS POSSIBLE

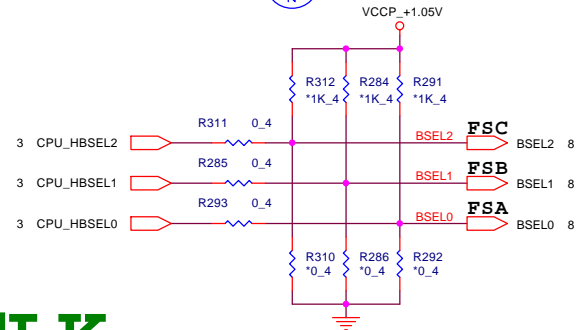
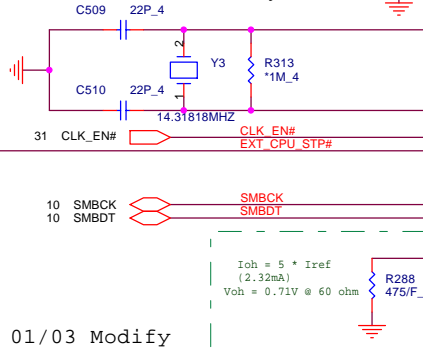
2- ROUTE ALL CPUCLK/#, NBCLK/# AND
ITPCLK/# AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U16
POWER PIN

```



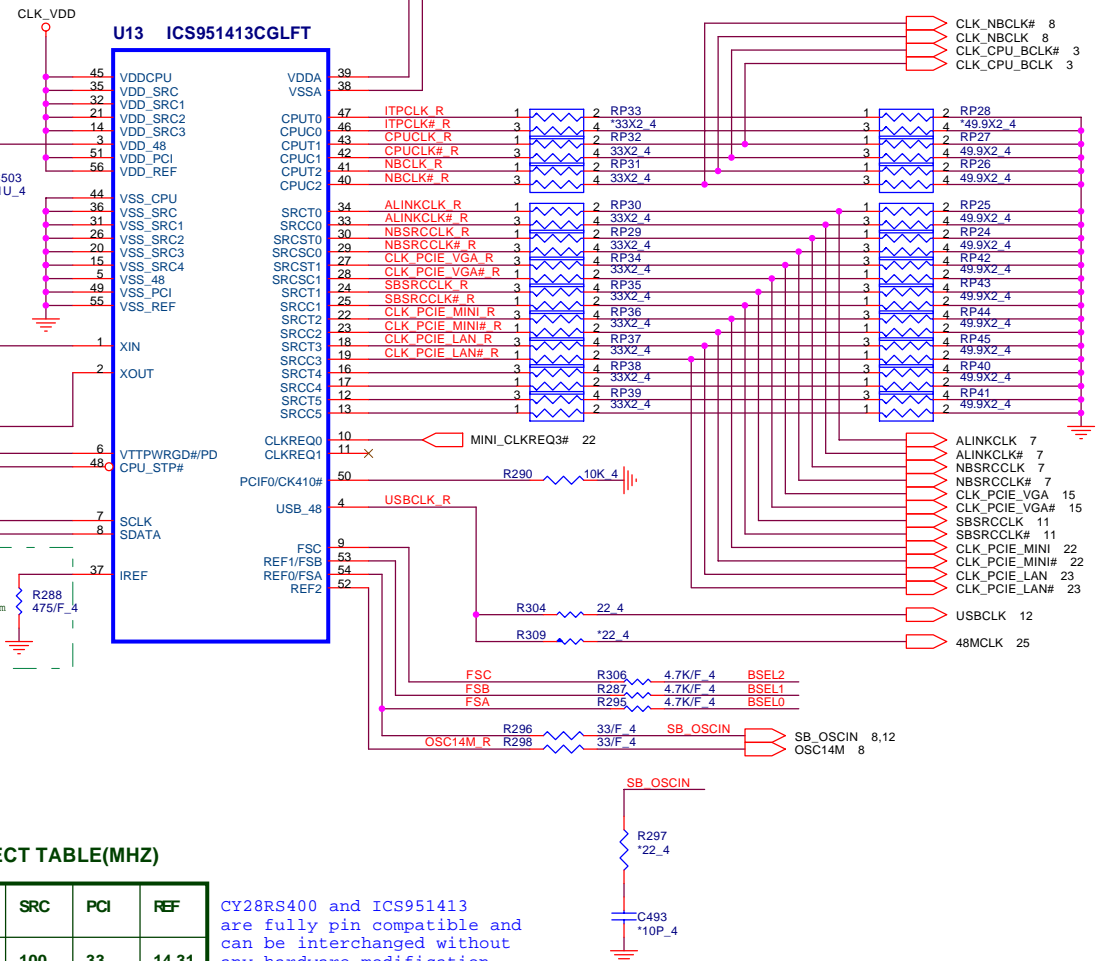
## Parallel Resonance Crystal



### CK410 FREQUENCY SELECT TABLE(MHZ)

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

CY28RS400 and ICS951413  
are fully pin compatible and  
can be interchanged without  
any hardware modification.



# CLK



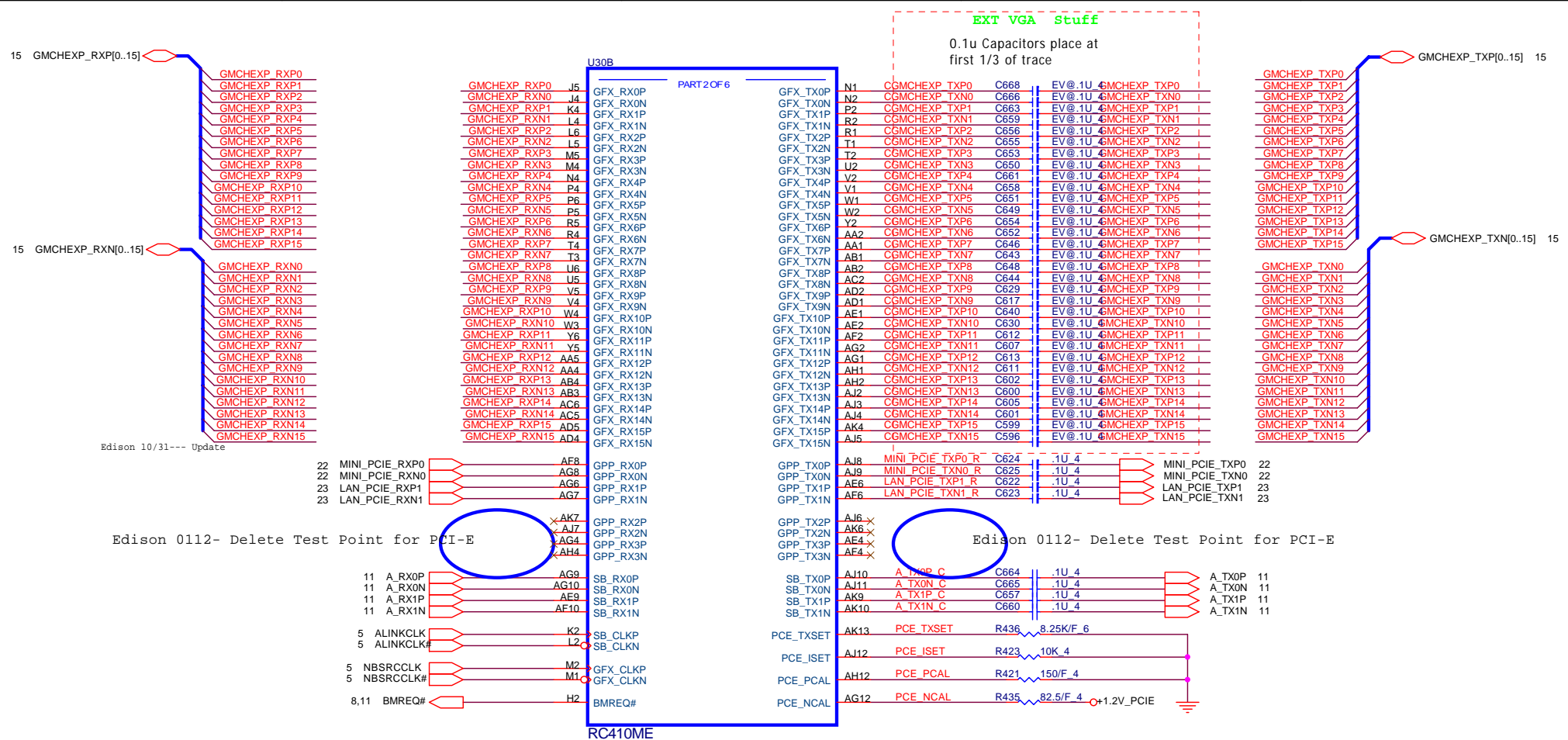
PROJECT : ZB3  
Quanta Computer Inc.


Size	Document Number	Rev
	<b>CLOCK GENERATOR</b>	1A
Date:	Monday, April 03, 2006	Sheet 5 of 37





NB-2





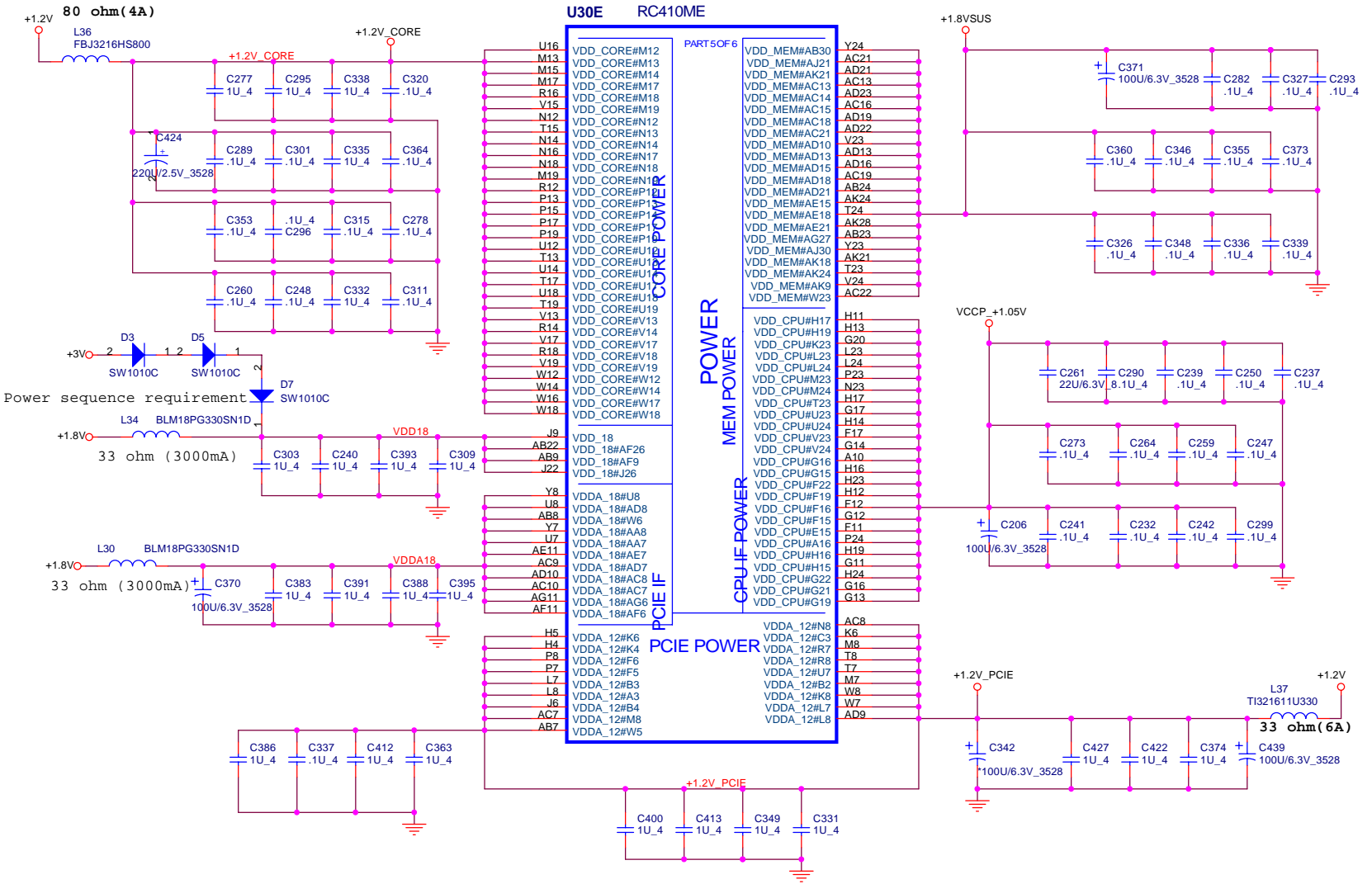
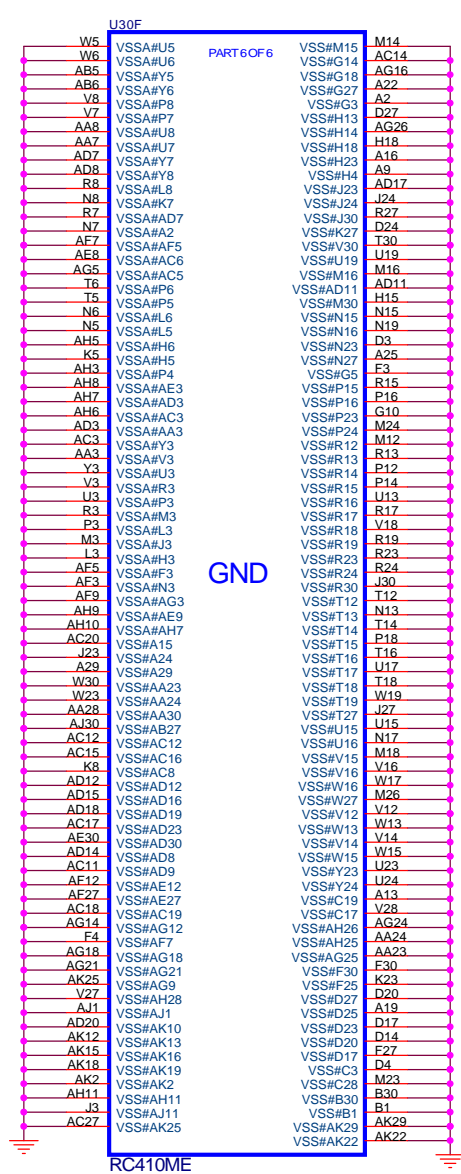
PROJECT : ZB3  
Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-PCIE LINK I/F	1A
Date:	Monday, April 03, 2006	Sheet 7 of 37





# NB-4



**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RC410MB-POWER</b>	1A

Date: Monday, April 03, 2006 Sheet 9 of 37

# DDR II

CLOCK 0,1  
CKE 0,1  
(NORMAL)

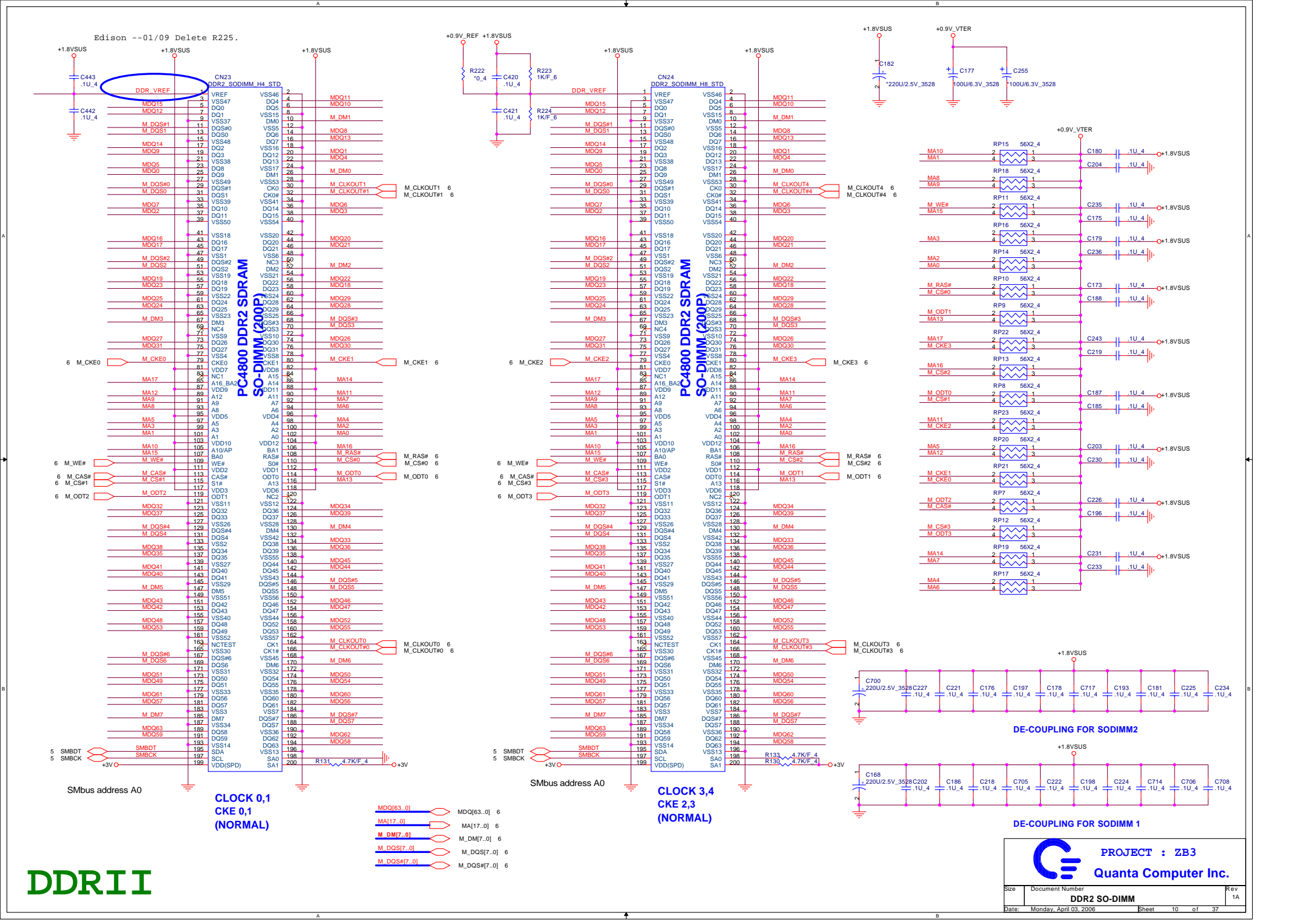
MDQ[63..0] 6  
MA[17..0] 6  
M\_DM[7..0] 6  
M\_DQS[7..0] 6  
M\_DQS#7[0] 6

CLOCK 3,4  
CKE 2,3  
(NORMAL)

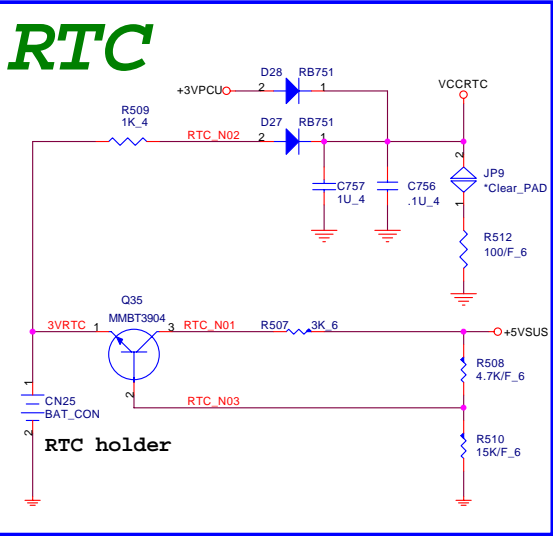
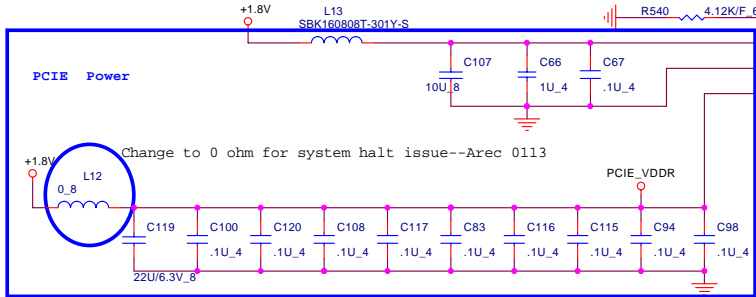
DE-COUPLING FOR SODIMM 1



PROJECT : ZB3  
Quanta Computer Inc.

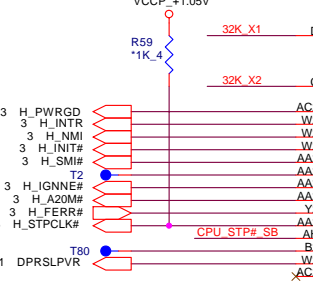
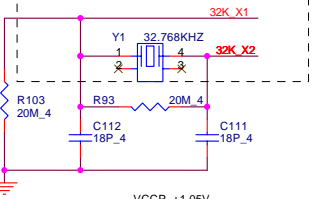


	SB CALIBRATION RESISTOR VALUE	
	SB600	SB460
R541	562 OHM 1%	150 OHM 1%
R543	2.05K 1%	150 OHM 1%
R540	0 ohm	4.12K 1%

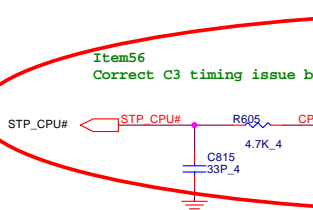


SB-1

ATI Recommend  
Vendor: NSK  
Part Number: NXG 32.768KAE12FUD 16 PPM



Item56  
Correct C3 timing issue by ATI recommend-- Arec 0215



## SB460 SB 27x27mm

Part 1 of 4

## PCI EXPRESS INTERFACE

## PCI INTERFACE

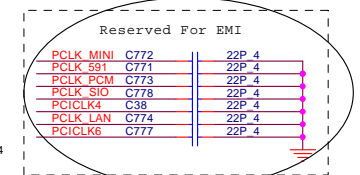
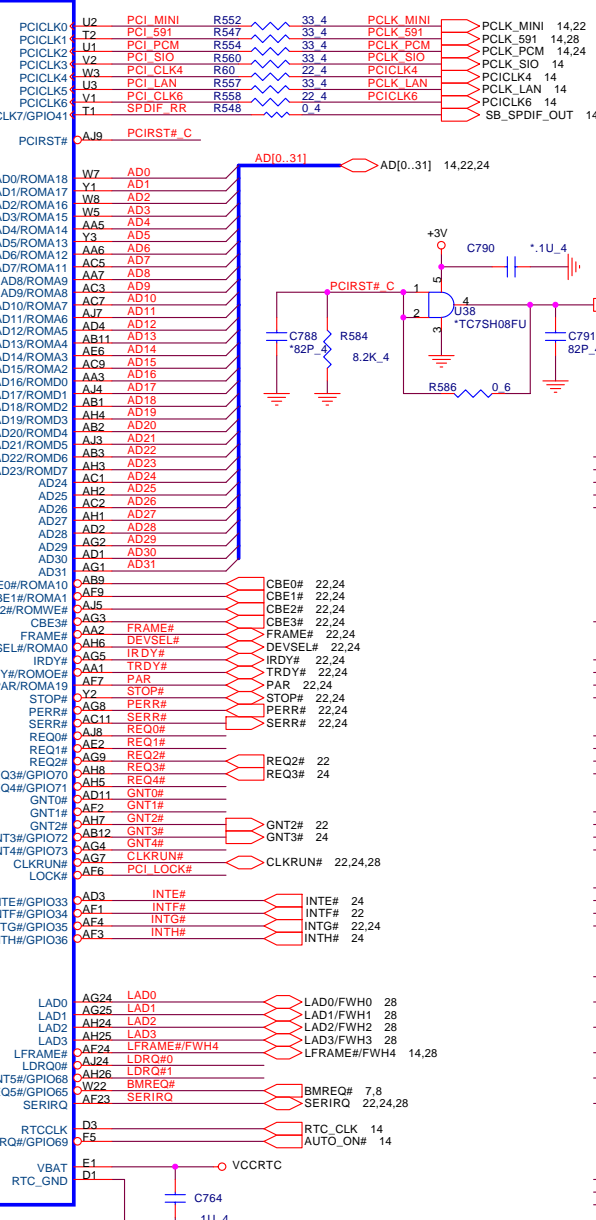
## LPC

## CPU

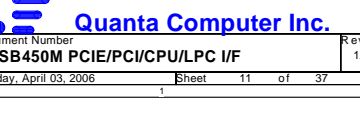
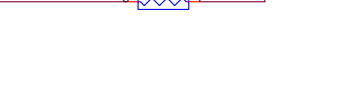
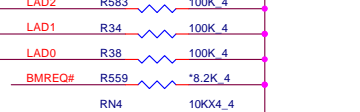
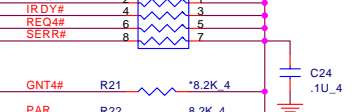
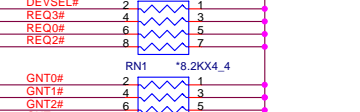
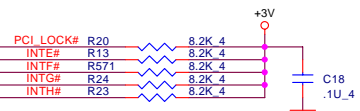
## RTC

## XTAL

## SB460



Edison - Feb/27 - The EMI  
recommend to install  
decoupling capas for the  
PCI Clock.  
Richard 3/8 -- From 33P\_4  
Change to 22P\_4

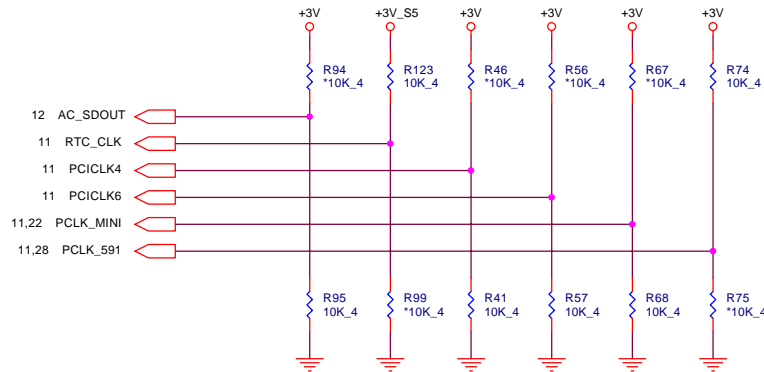






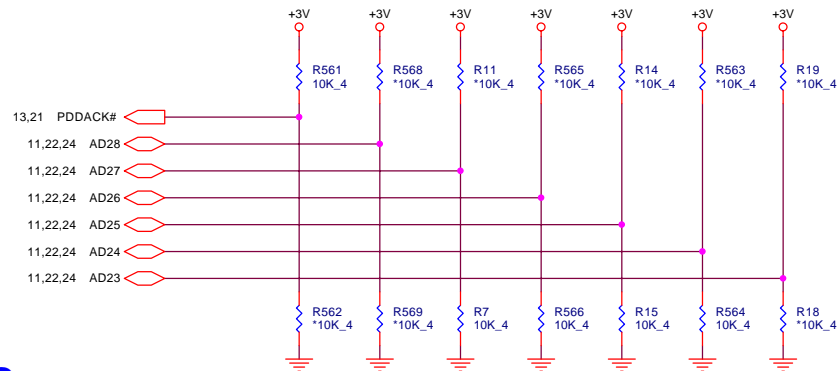


## REQUIRED STRAPS

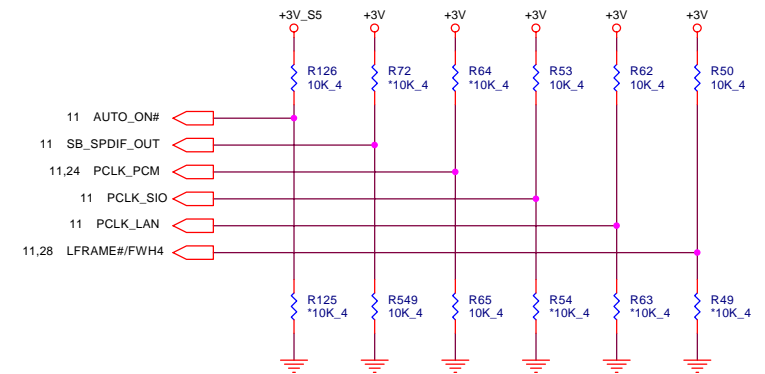


					PCLK_MINI	PCLK_591
PULL HIGH	AC_SDOUT USE DEBUG STRAPS	RTC_CLK INTERNAL RTC DEFAULT	PCI_CLK4 USE INT. PLL48	PCI_CLK6 CPU IF=K8	PCI_CLK0	PCI_CLK1
					ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM L, L = FWL ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT		

Edison-11/07-- Modify



	PDDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	



	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
PULL HIGH	ACPWRON MANUAL PWR ON DEFAULT	SPDIF_OUT SIO 24MHz	PCI_CLK2 XTAL MODE NOT SUPPORTED	PCI_CLK3 USB PHY POWERDOWN DISABLE DEFAULT	PCI_CLK5 PCIE_CM_SET LOW DEFAULT	LFRAME# ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#


## DEBUG STRAPS

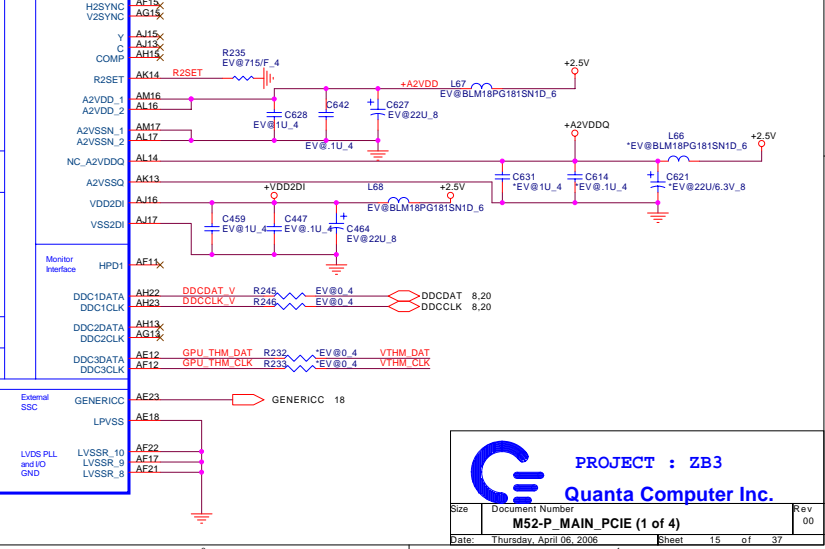
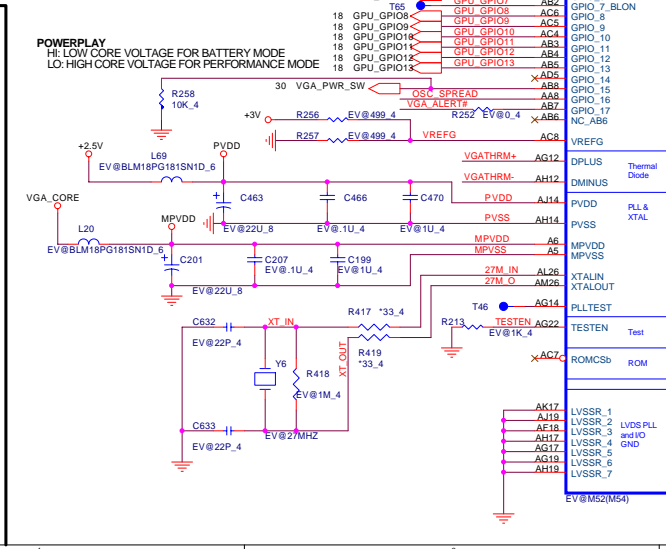
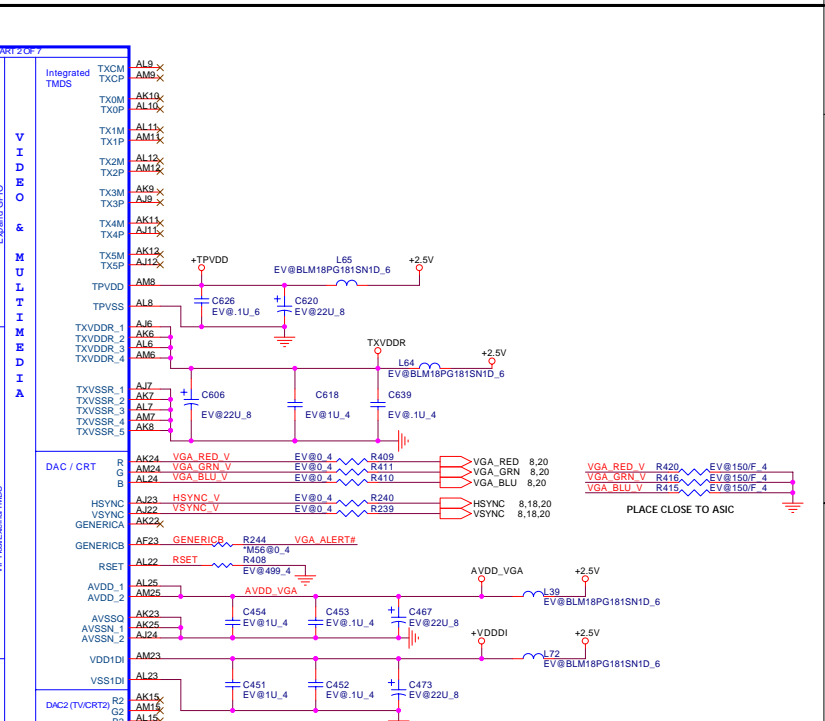
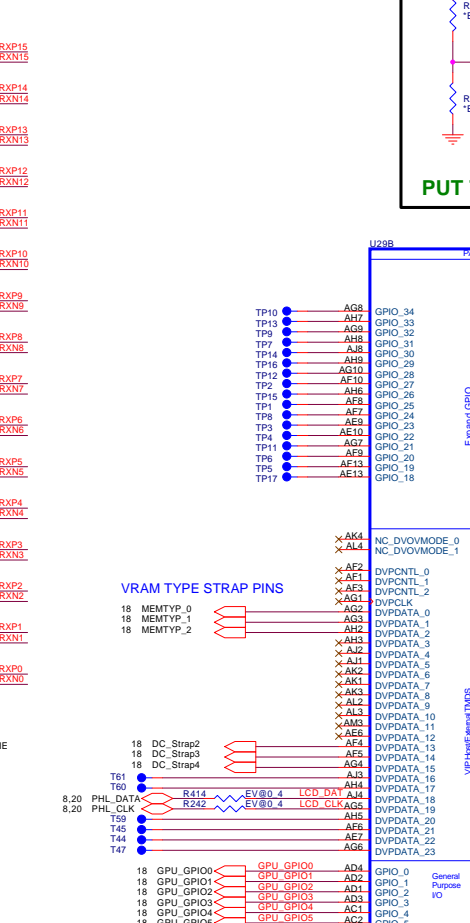
SB-4

PROJECT : ZB3  
Quanta Computer Inc.

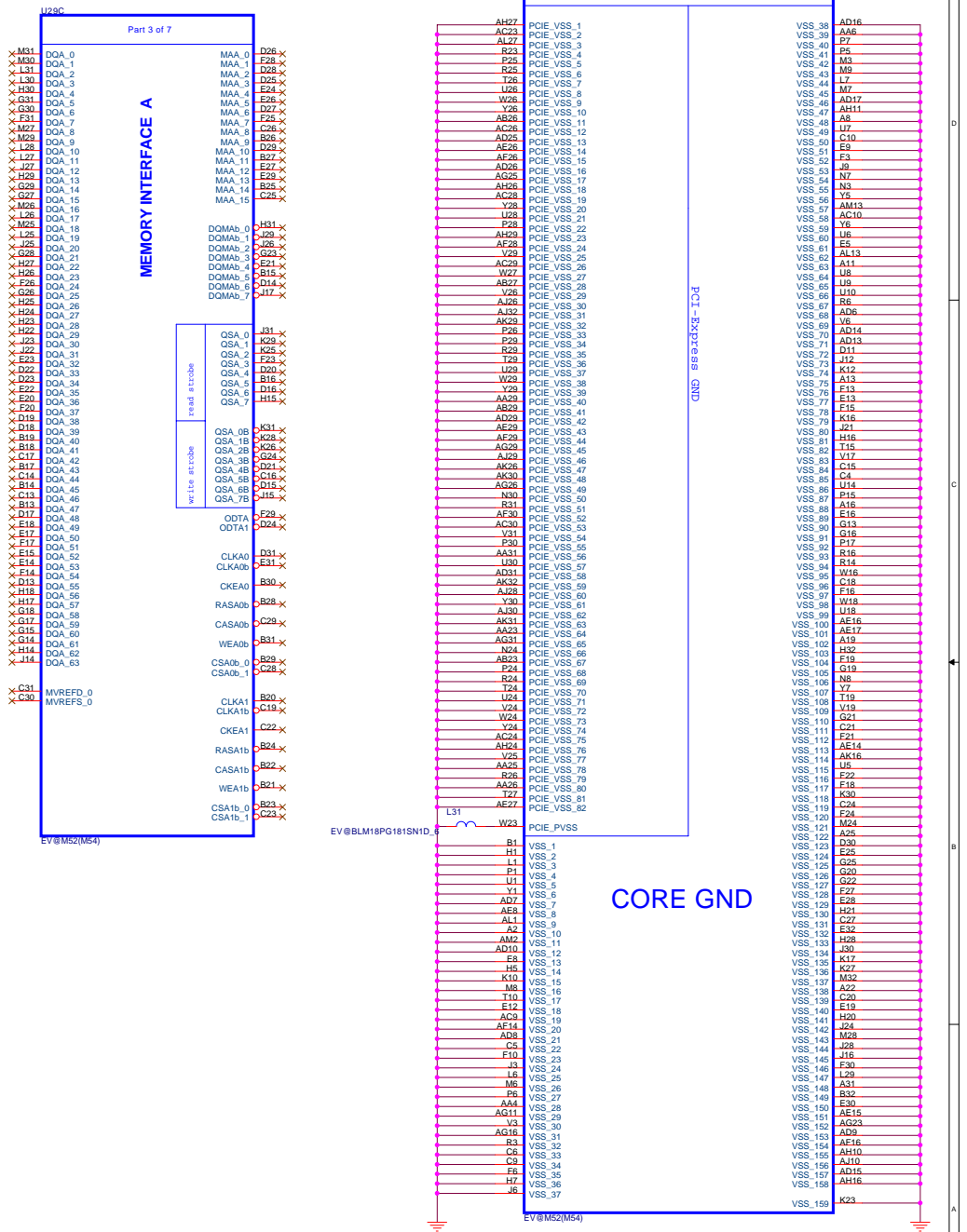
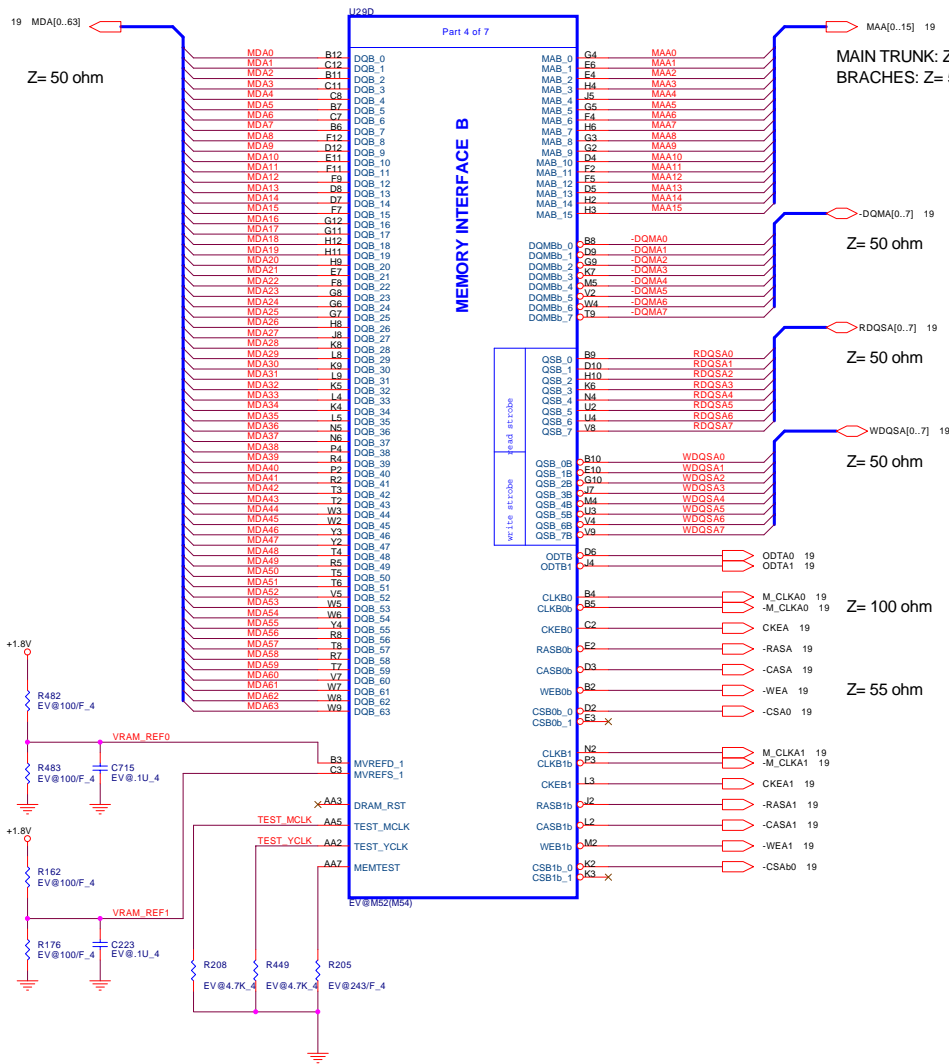
Size Custom	Document Number SB450M STRAPS	Rev 1A
Date: Monday, April 03, 2006	Sheet 14 of 37	



7 GMCHEXP\_TXP[0..15] 

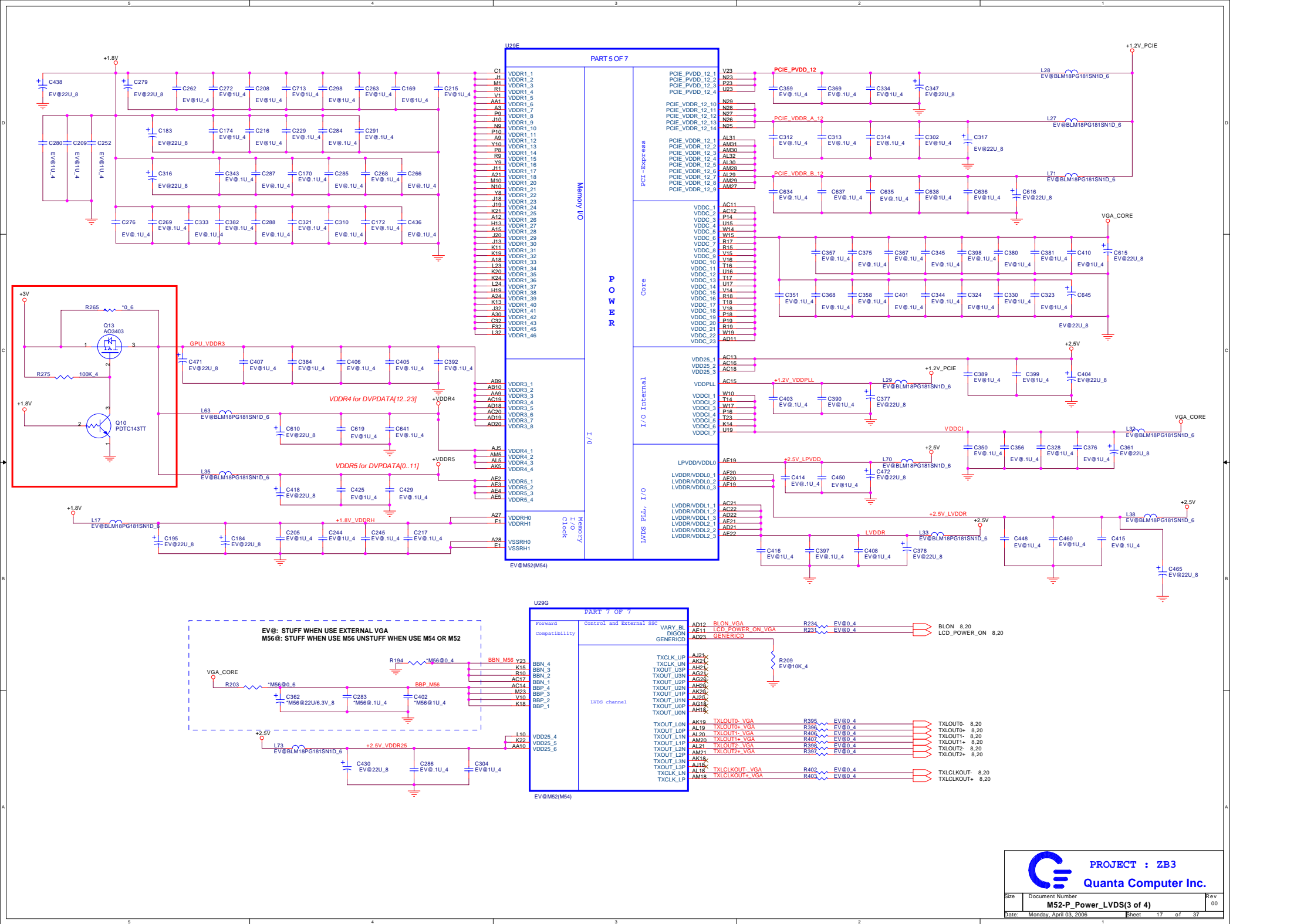


## RV410 MEMORY CHANNELS A and B



PROJECT : ZB3  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>M52-P_MEM_GND (2 of 4)</b>	00
Date:	Monday, April 03, 2006	Sheet 16 of 37



Overlap pads to save space  
and to prevent assembly of  
both resistors.

#### Layout



Ground  
↓  
High logic voltage  
Signal

Add Text "Populate to Enable Debug"  
Beside JU23 on Silkscreen.

Vendor	P/N	QCI	P/N	Size	GPU_GPIO13	GPU_GPIO12	MEMTYP_1	MEMTYP_0
HYB18T256161AFL25	AKD5JG-T*08	16M*16	*4pcs	(128MB)	0	0	0	0
HY5PS561621AFP-25	AKD5JG-TW12	(Default setting)						
K4N56163QG-ZC25	AKD5JG-T514							
HYB18T512161BF-25	AKD5FG-T*00	32M*16	*2pcs	(128MB)	0	0	1	1
HY5PS121621BFP-25	AKD5FG-TW14							
K4N51163QC-ZC25	AKD5FGBT501	32M*16	*4pcs	(256MB)	0	1	0	1

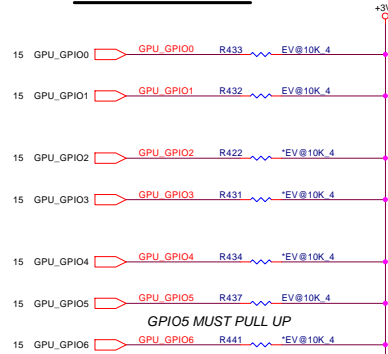
#### Memory Aperture Size Select

When no ROM is attached, GPIO\_9 is set to 0  
GPIO\_13:12 is used to select the memory aperture size.  
GPIO\_13:12 = 00: 128M memory aperture, same as ROM strap 00  
GPIO\_13:12 = 01: 256M memory aperture, same as ROM strap 01  
GPIO\_13:12 = 10: 64M memory aperture, same as ROM strap 10  
GPIO\_13:12 = 11: reserved, same as ROM strap 11

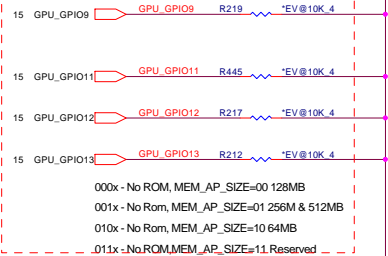
Default: 128M memory aperture.

GPIO\_13:12 = 01 (256M memory aperture) recommended  
for designs with 256MB or 512MB of physical memory.

## OPTION STRAPS



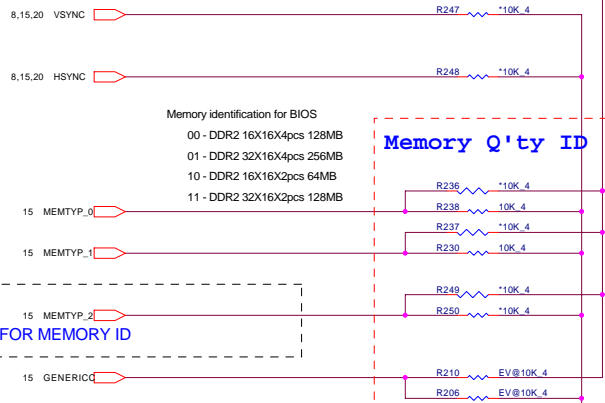
## Memory Size strap



#### Memory identification for BIOS

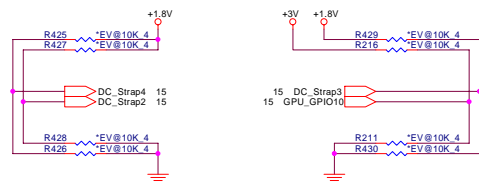
- 00 - DDR2 16X16X4pcs 128MB
- 01 - DDR2 32X16X4pcs 256MB
- 10 - DDR2 16X16X2pcs 64MB
- 11 - DDR2 32X16X2pcs 128MB

## Memory Q'ty ID



## RESERVE FOR MEMORY ID

#### ATI FAE: ALL N/A



## M56-P Strap

STRAPS	PIN	DESCRIPTION	Board DEFAULT
TX_PWRS_ENB	GPIO0 (Internal pull-down)	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	1
TX_DEEMPH_EN	GPIO1 (Internal pull-down)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	1
	GPIO(3:2) (Internal pull-down)	RSVD	
DEBUG_ACCESS	GPIO4 (Internal pull-down)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5 (Internal pull-down)	RSVD	
	GPIO6 (Internal pull-down)	RSVD	
Force_ Compliance	GPIO8 (Internal pull-down)	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13,12,11) (Internal pull-down)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128M 001x - No Rom, MEM_AP_SIZE=01 256M 010x - No Rom, MEM_AP_SIZE=10 64M 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	000
VIP_DEVICE	VSYN	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYN, V2SYN, GENERIC	RSVD	
	VSYN	RSVD	
	HSYN	RSVD	
	PCIE_TEST	RSVD	

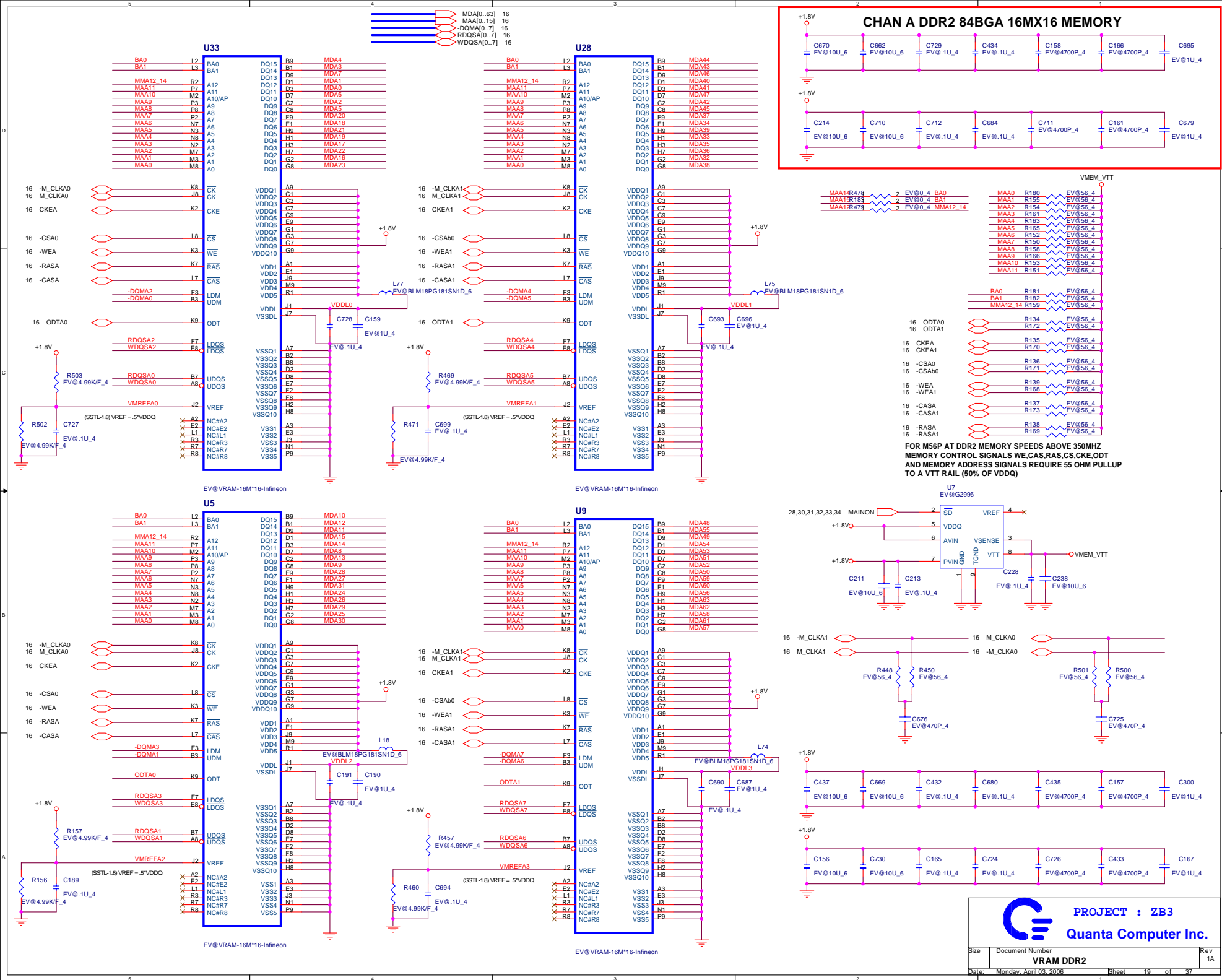
## Board Straps

REV. 0.3

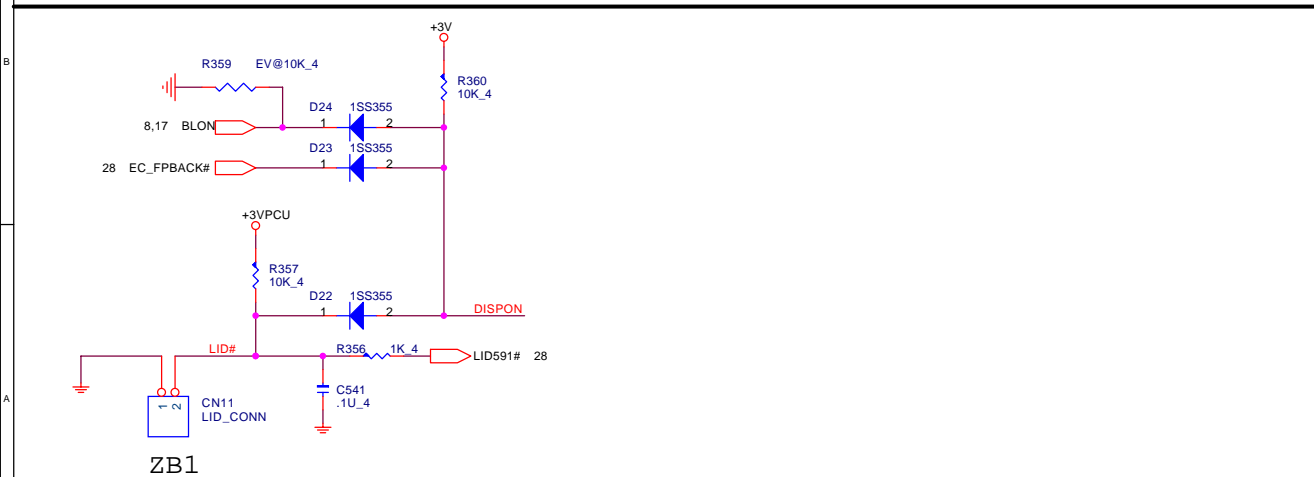
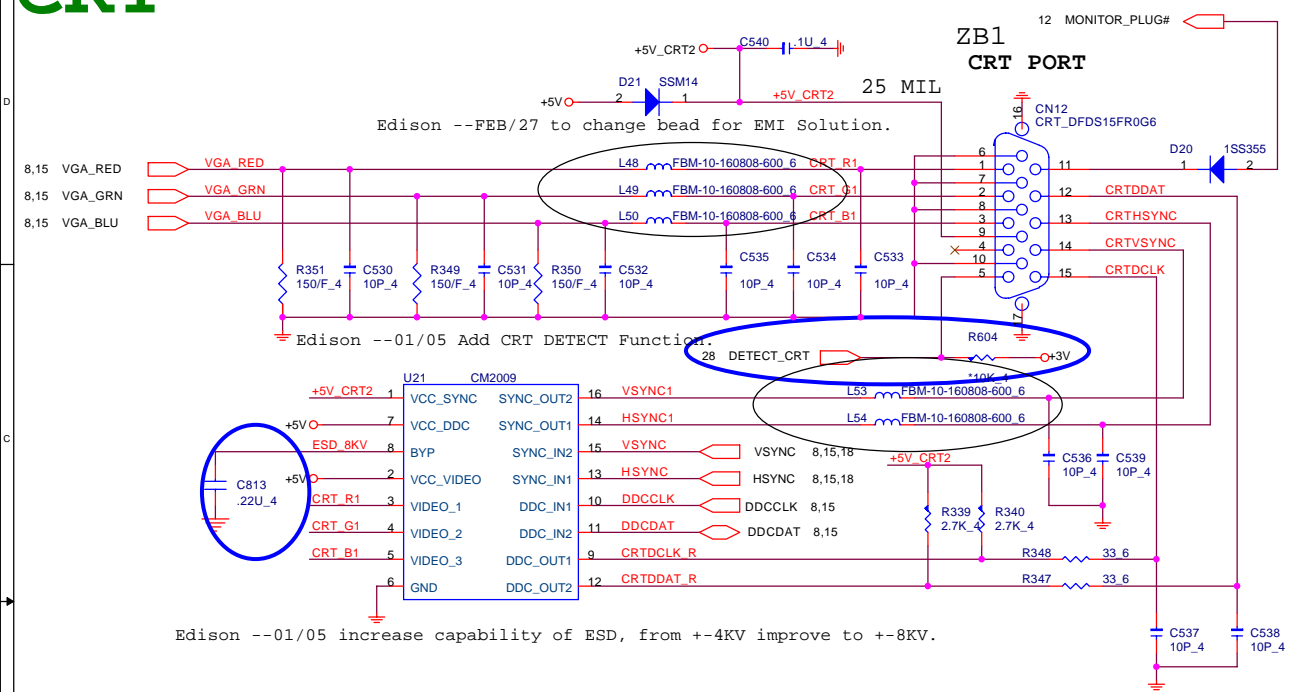
STRAPS	PIN	DESCRIPTION	VALUE
MEMTYP(1:0)	DVPDATA(1:0)	Memory identification for BIOS 00 - DDR2 16X16X4pcs 128MB 01 - DDR2 32X16X4pcs 256MB 10 - DDR2 16X16X2pcs 64MB 11 - DDR2 32X16X2pcs 128MB	
DC_Strip1	GPIO(10)	Internal TMSD Enabled 0 - Disabled 1 - Enabled	1
DC_Strip2	DVPDATA13	Video Capture Enabled 0 - Disabled 1 - Not detected	0
DC_Strip3	DVPDATA14	HDTV out detect 0 - Detected 1 - Enabled	1
DC_Strip4, DEMUX_SEL	DVPDATA15	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TV0 Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1



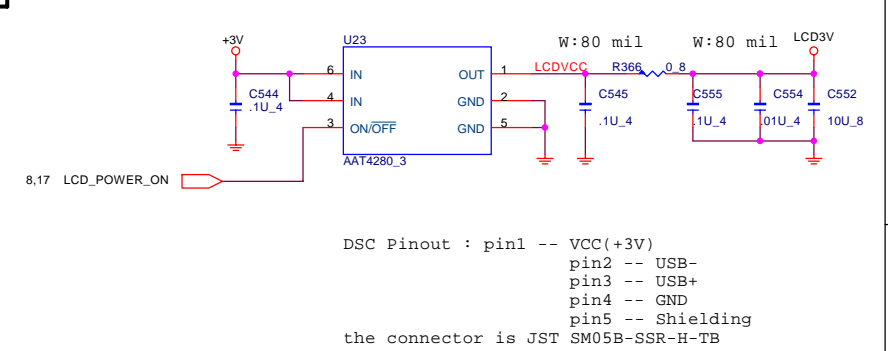
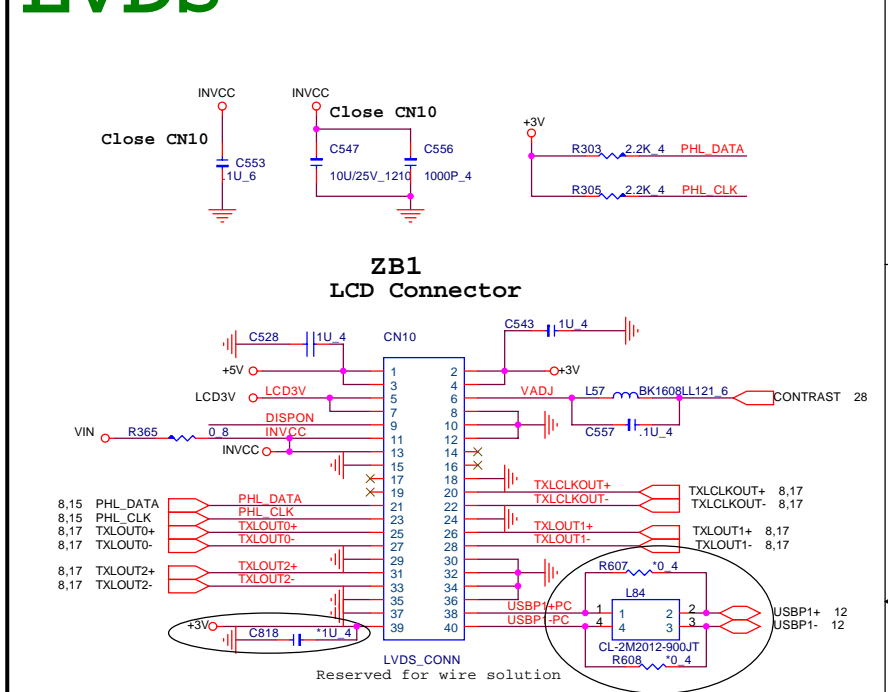
PROJECT : ZB3  
Quanta Computer Inc.




# CRT



# LVDS



DSC Pinout : pin1 -- VCC(+3V)  
 pin2 -- USB-  
 pin3 -- USB+  
 pin4 -- GND  
 pin5 -- Shielding  
 the connector is JST SM05B-SSR-H-TB

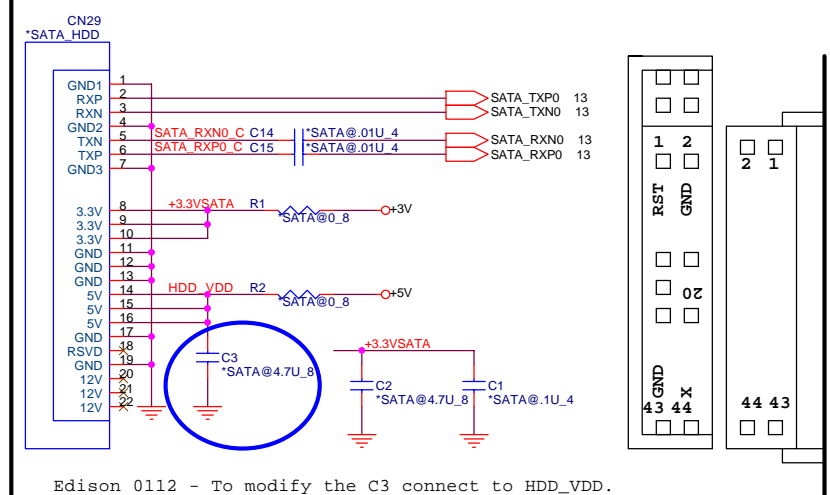
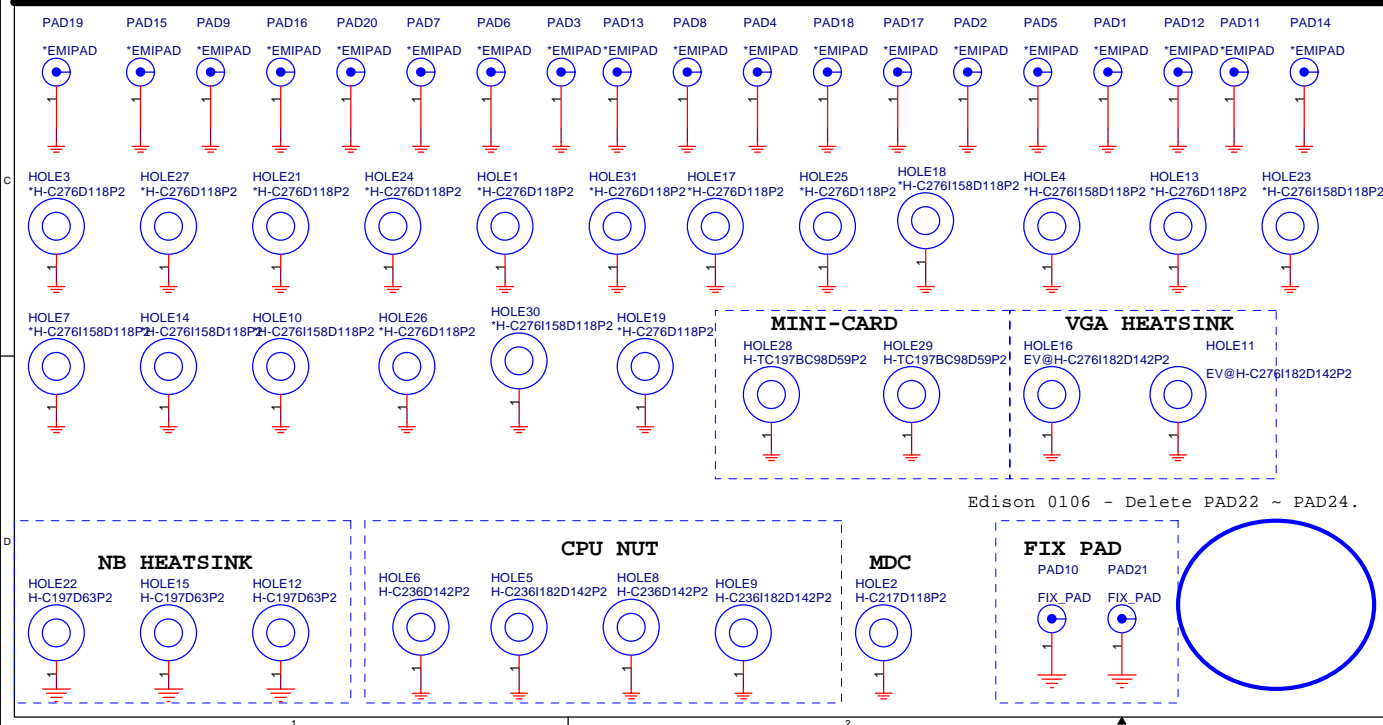
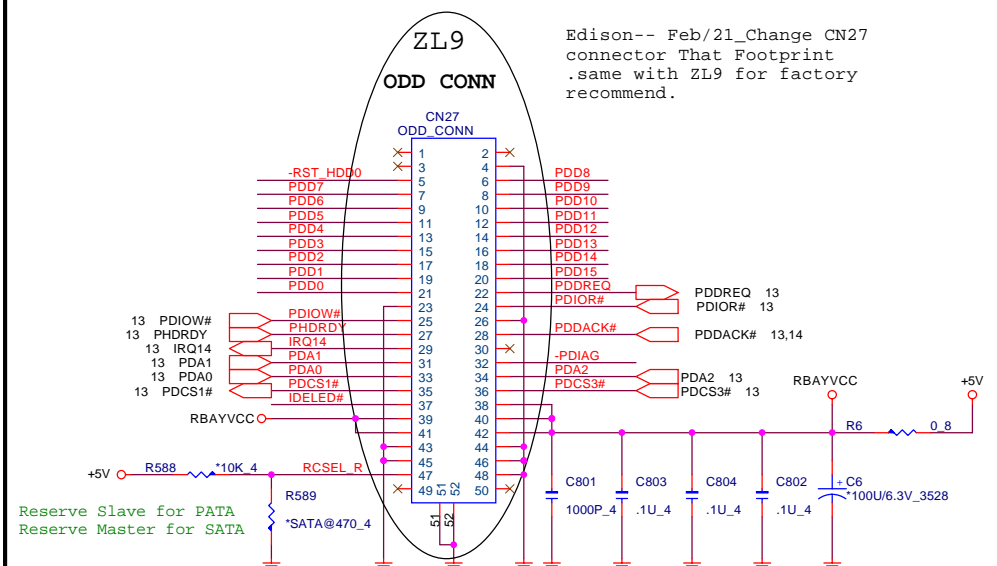
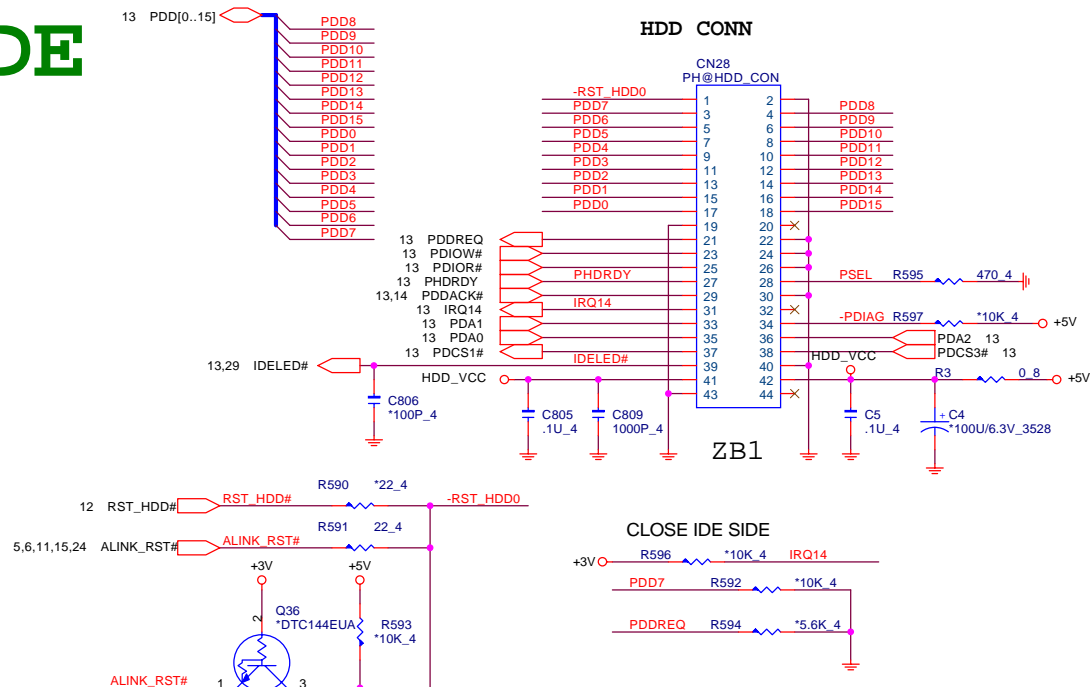


**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev 1A
<b>VGA Ports, LID, &amp; HOLES</b>		
Date:	Monday, April 03, 2006	Sheet 20 of 37



# IDE



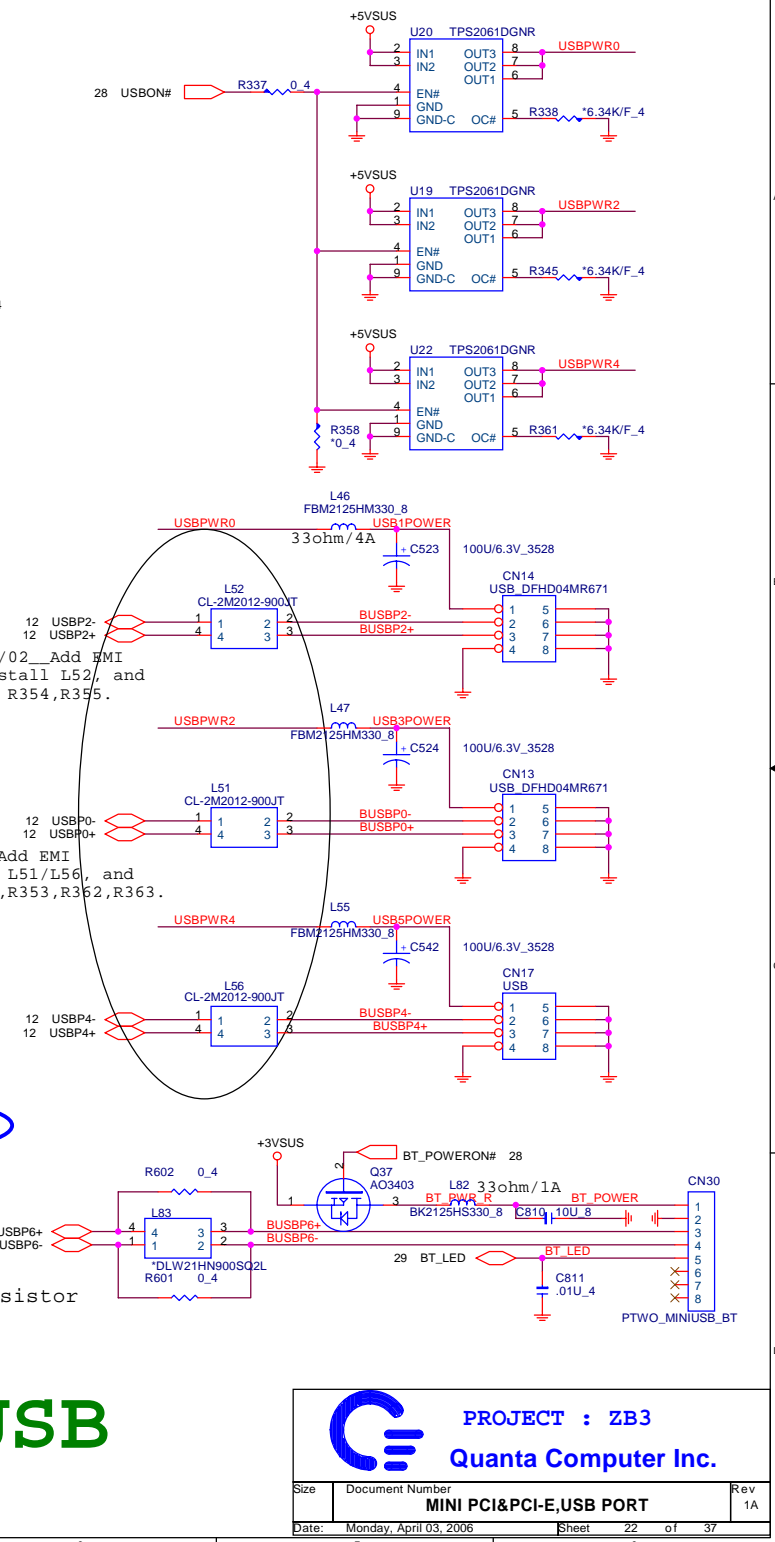
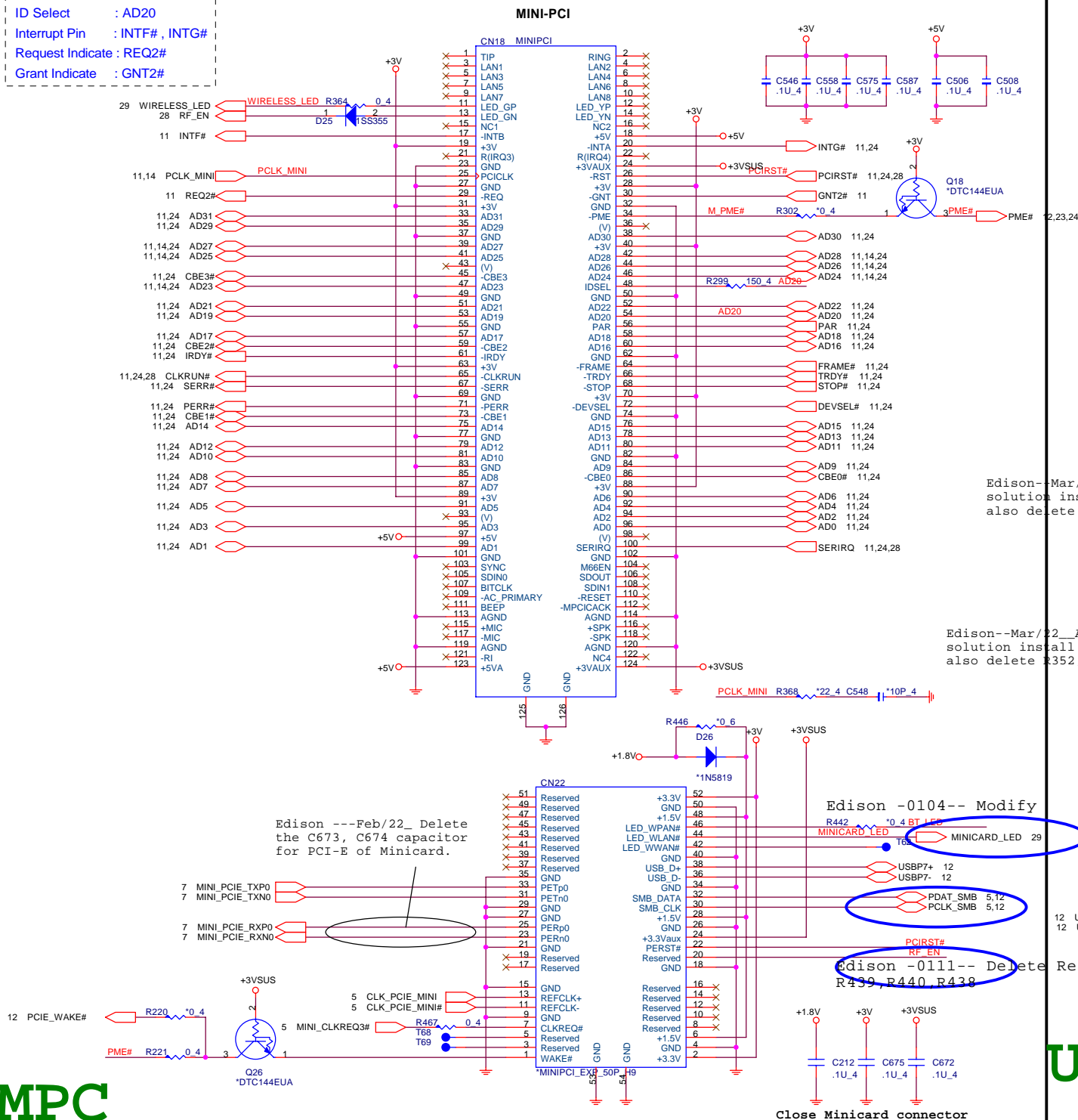
Edison 0112 - To modify the C3 connect to HDD\_VDD.



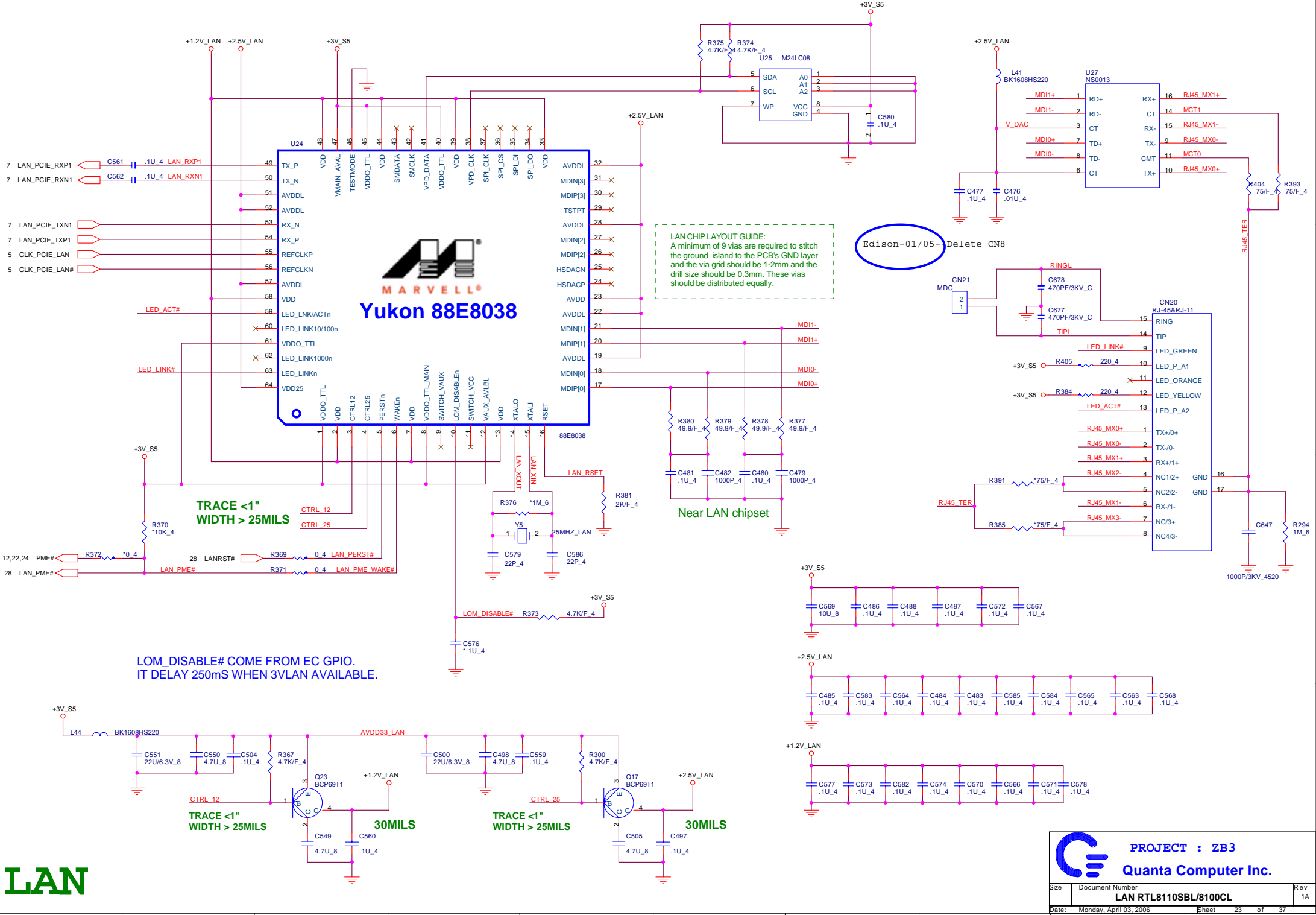
PROJECT : ZB3  
Quanta Computer Inc.

Size	Document Number <b>HDD &amp; CDROM , HOLES</b>	Rev <b>1A</b>
Date:	Monday, April 03, 2006	Sheet 21 of 37

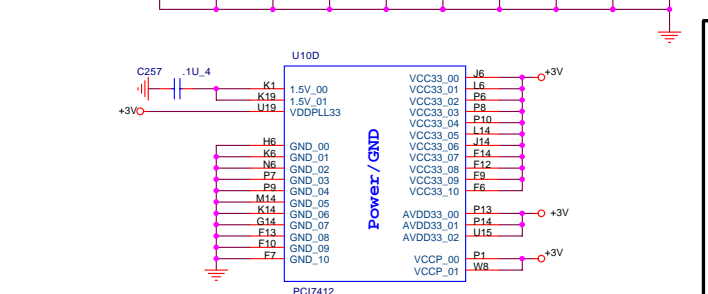
ID Select : AD20  
Interrupt Pin : INTF# , INTG#  
Request Indicate : REQ2#  
Grant Indicate : GNT2#



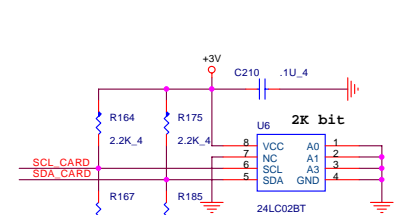
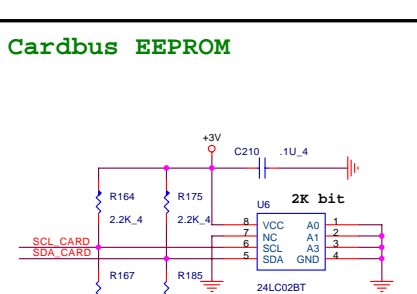
LAN



Timing diagram for AD17 showing signals GNT3#, REQ3#, FRAME#, IRDY#, DEVSEL#, TRDY#, SER#, STOP#, PER#, and PAR. The diagram shows a sequence of events where GNT3# and REQ3# are active low signals, and FRAME#, IRDY#, DEVSEL#, TRDY#, SER#, STOP#, PER#, and PAR are active low signals. A blue waveform labeled 'K188' is shown between REQ3# and FRAME#.

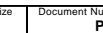
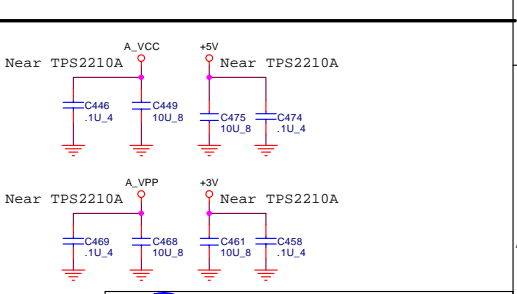
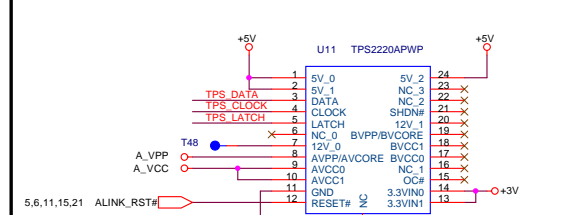


8	
---	--

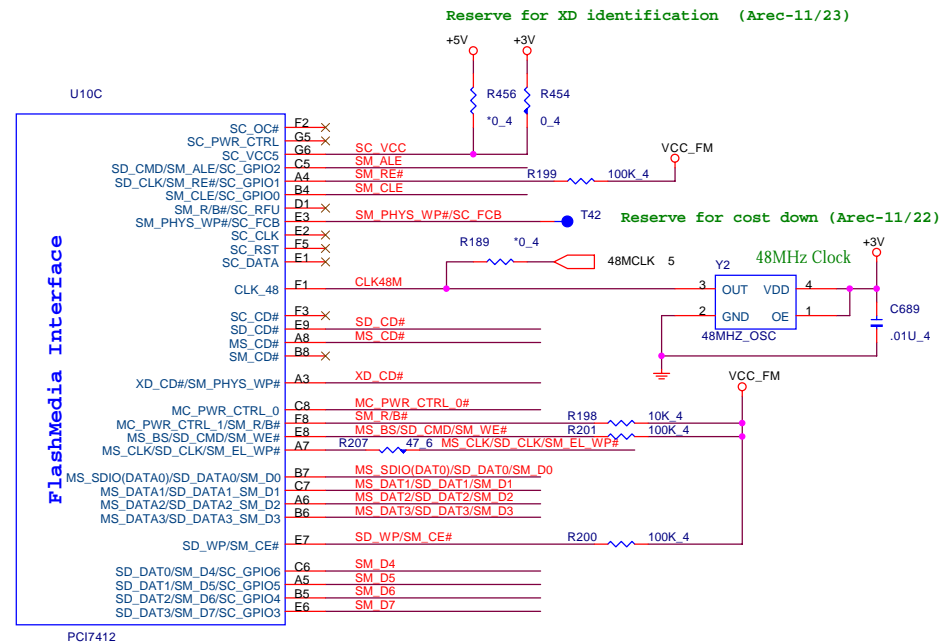


## Cardbus power switch

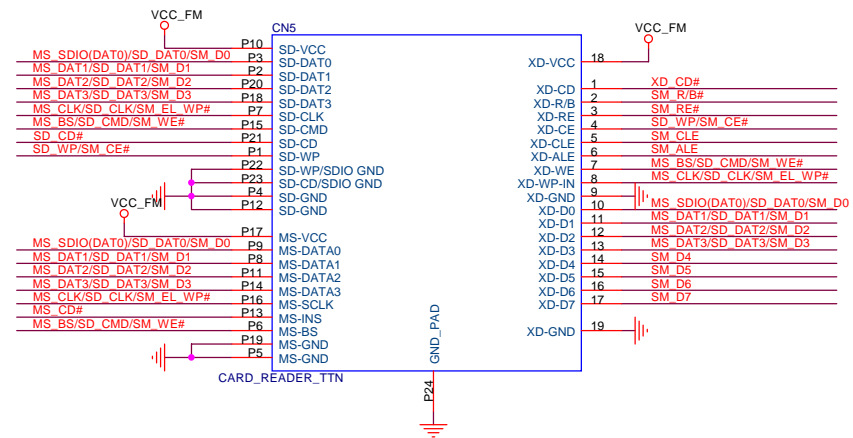
\_\_\_\_\_



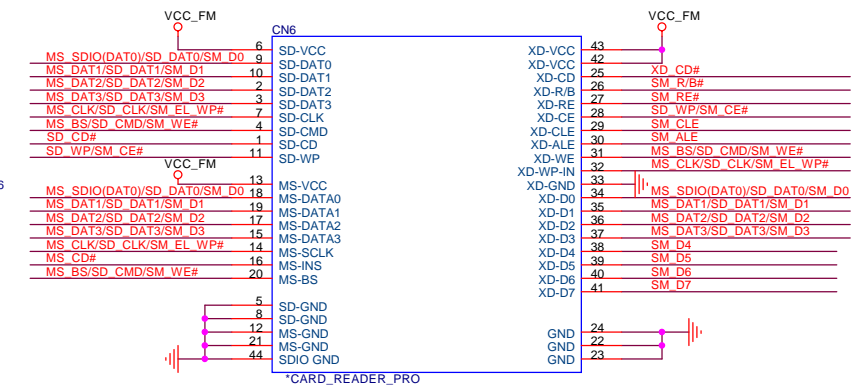
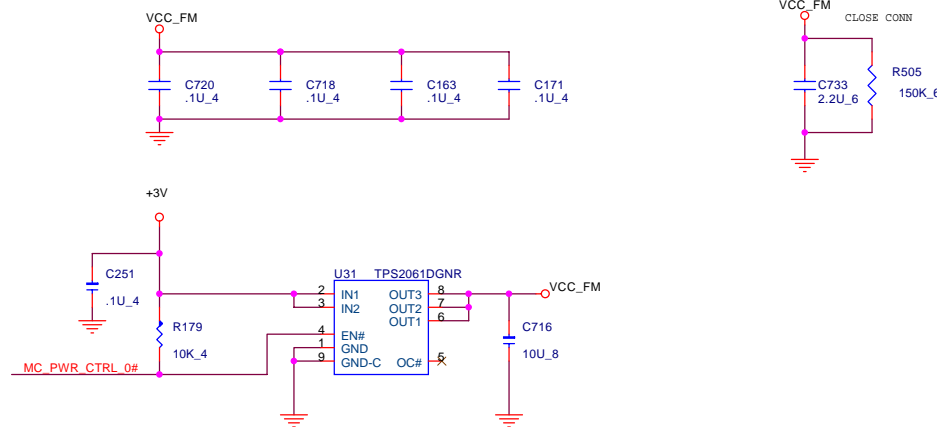
number	Rev
PCI7412-PCMCIA CONTROLLE	1A



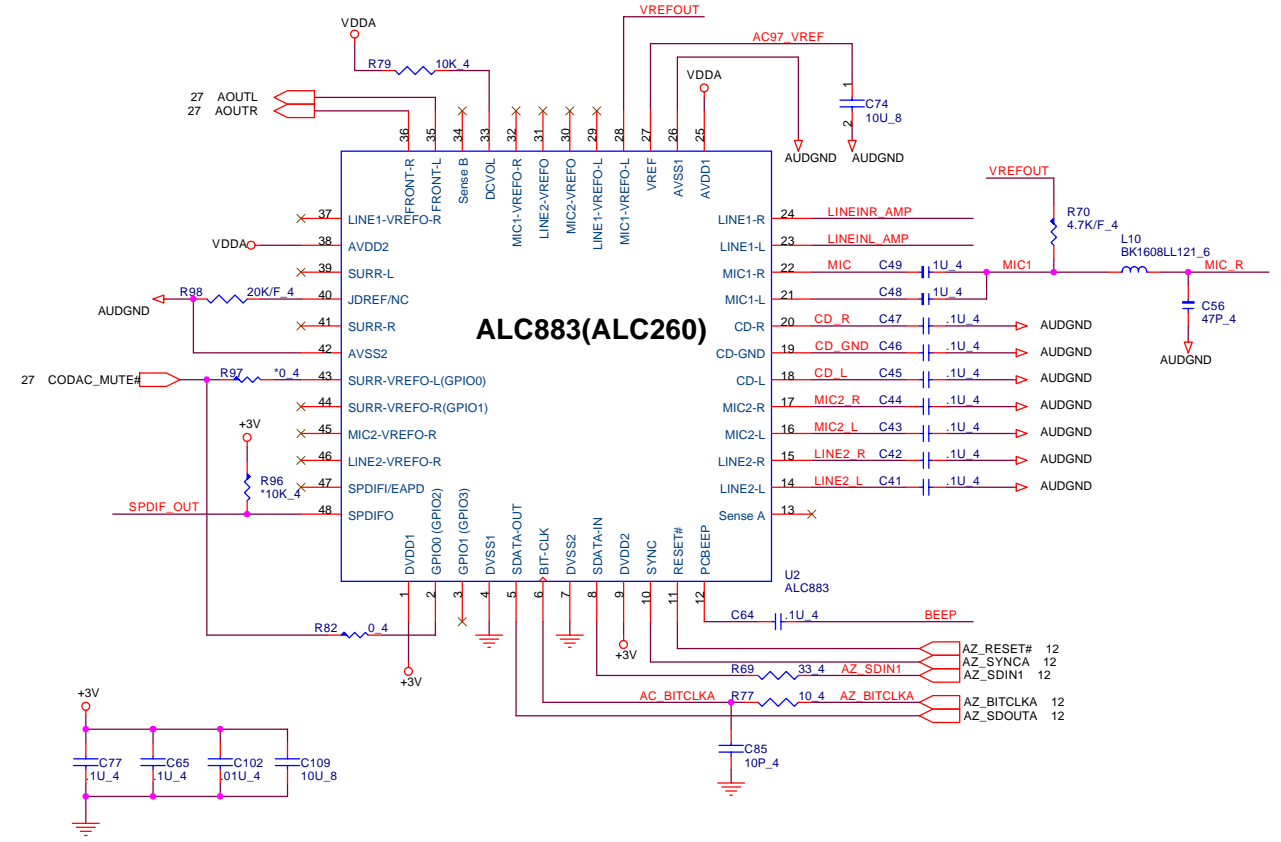
**DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.**



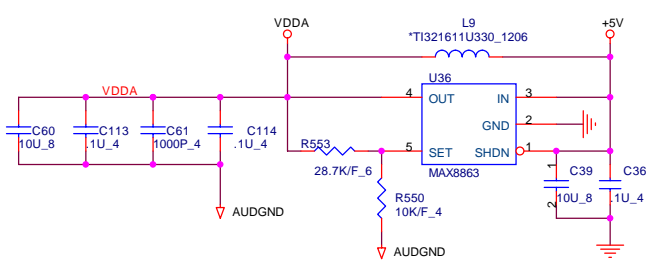
## 5 IN1 CARD READER



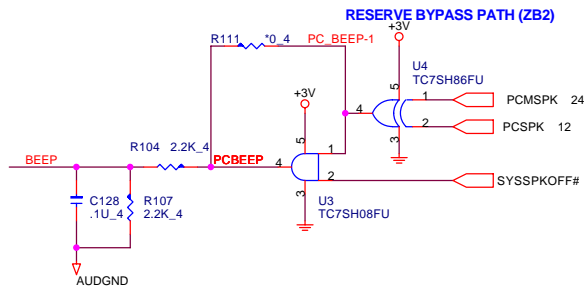
ADO



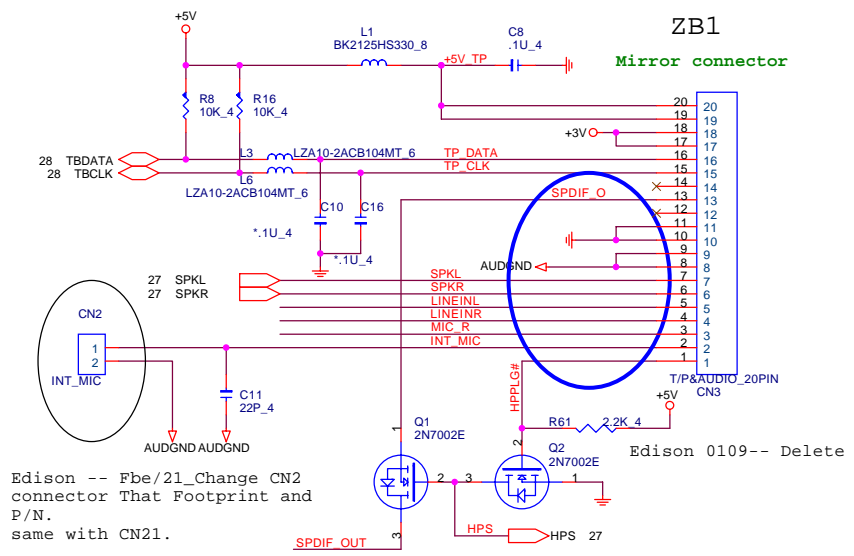
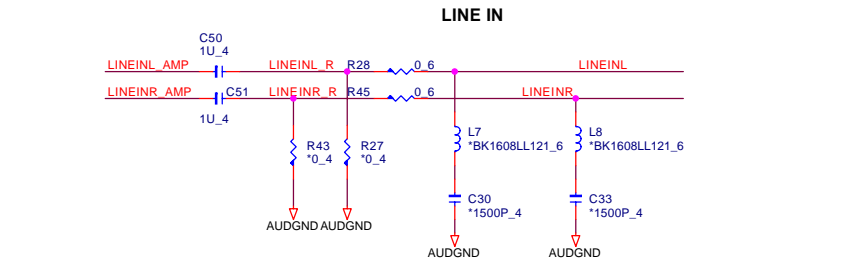
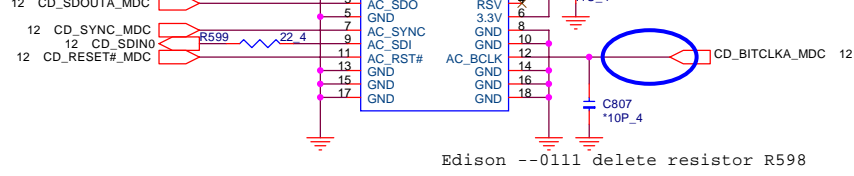
Audio Power



BEEP



MDC



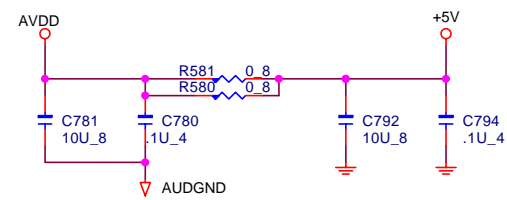
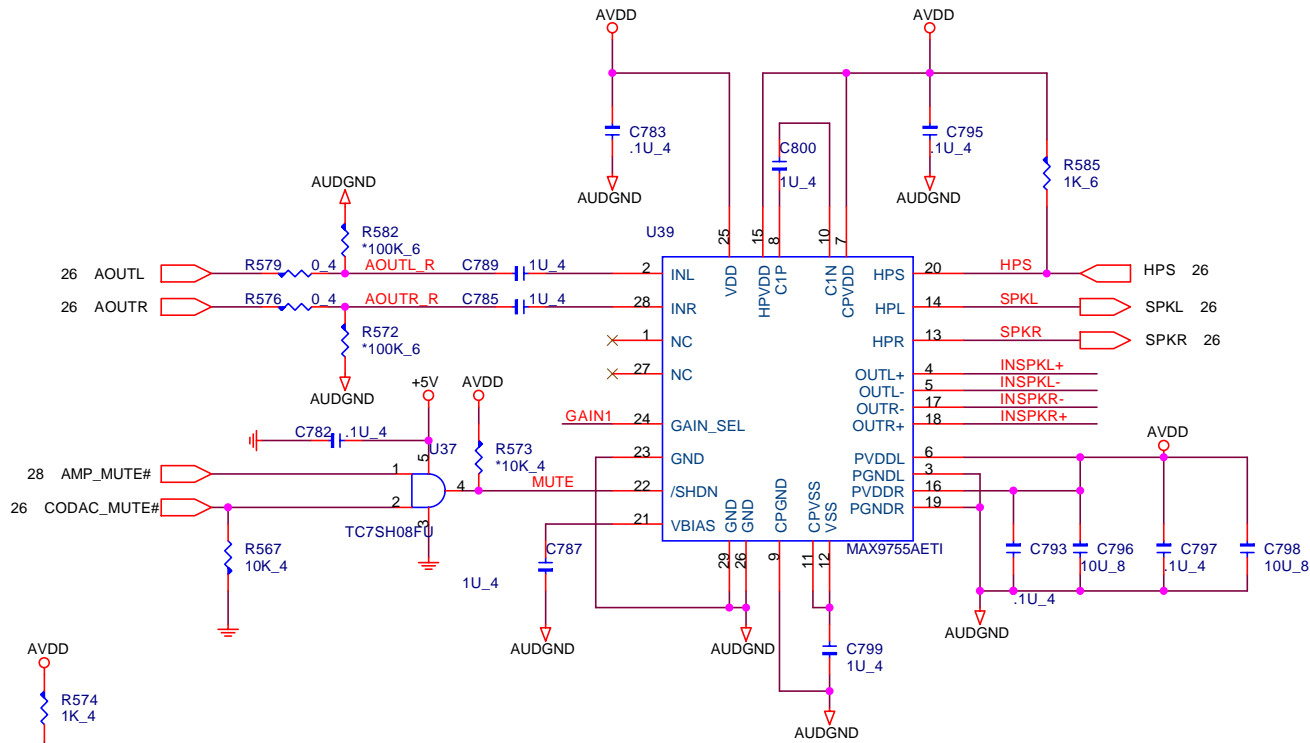
Edison -- Fbe/21\_Change CN2 connector That Footprint and P/N. same with CN21.

PROJECT : ZB3

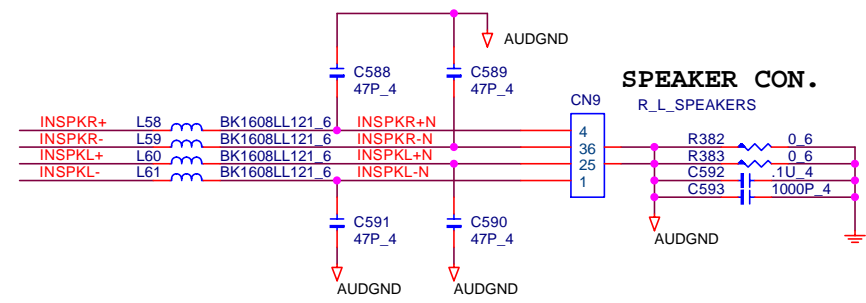
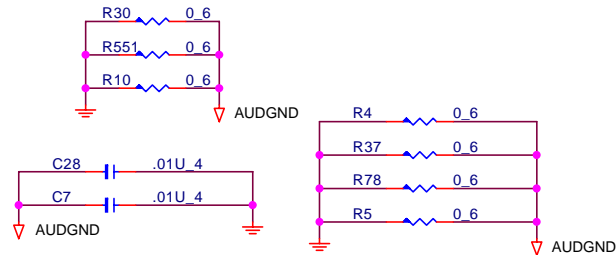
Quanta Computer Inc.

Size	Document Number	Rev
	CODEC & LINE IN & MIC	1A
Date:	Monday, April 03, 2006	Sheet 26 of 37






GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



AMP



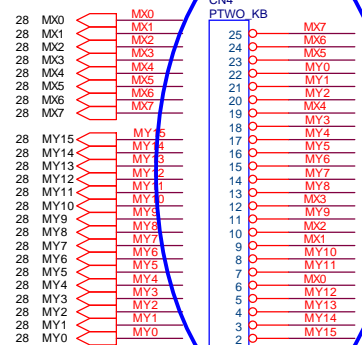
PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
	<b>AUDIO AMP</b>	1A
Date:	Monday, April 03, 2006	Sheet 27 of 37



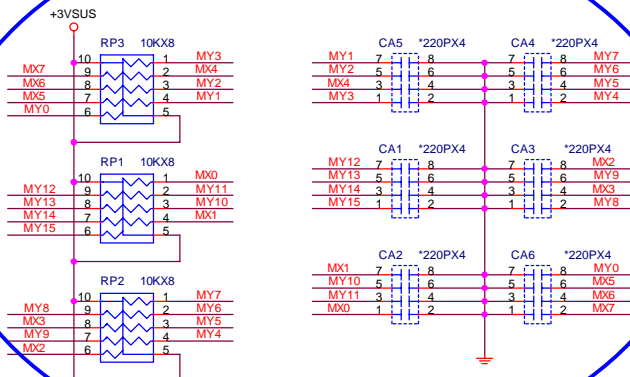
# INT K/B



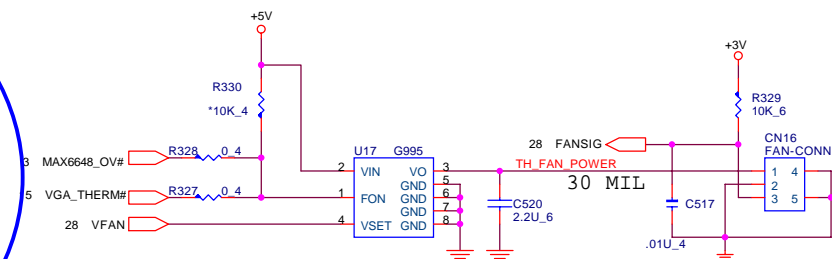
ZB1

Edison --01/03 Modify

Edison --01/04 Modify for pin swap



# FAN CONTROL

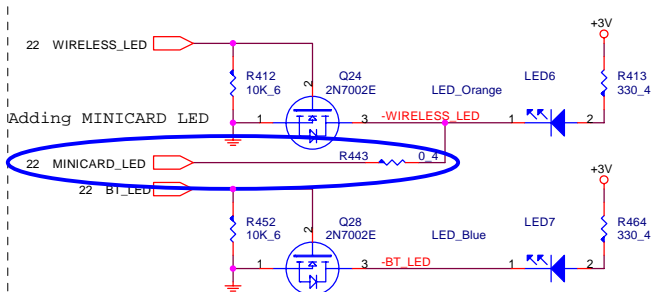
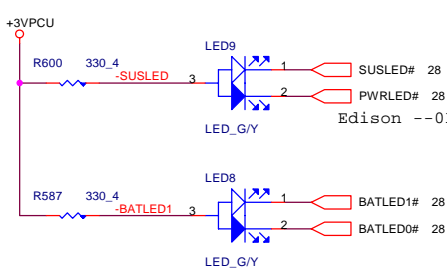
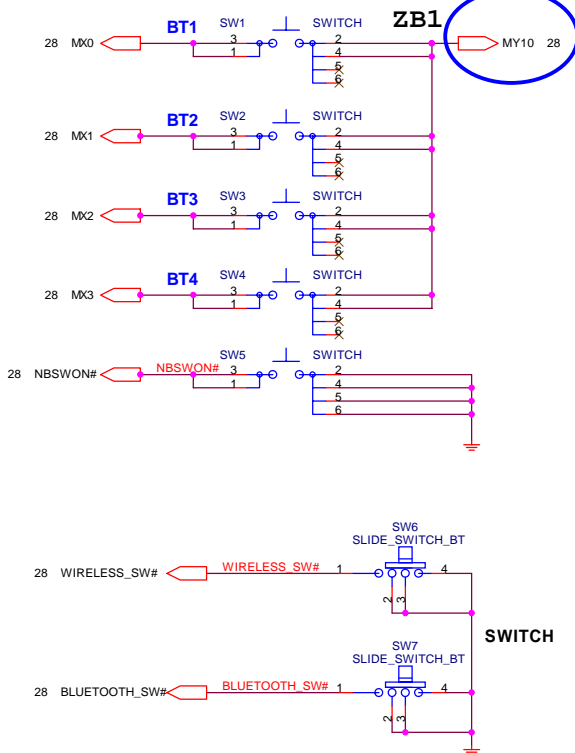


KBC

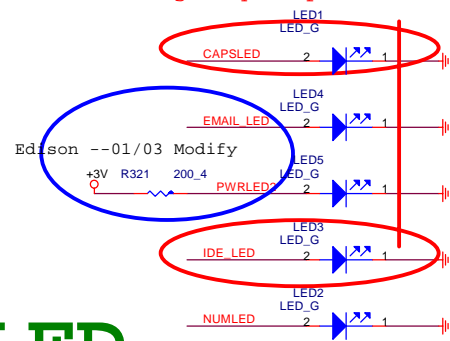
THM

Edison --01/04 Modify

Check color



Exchange Layout position

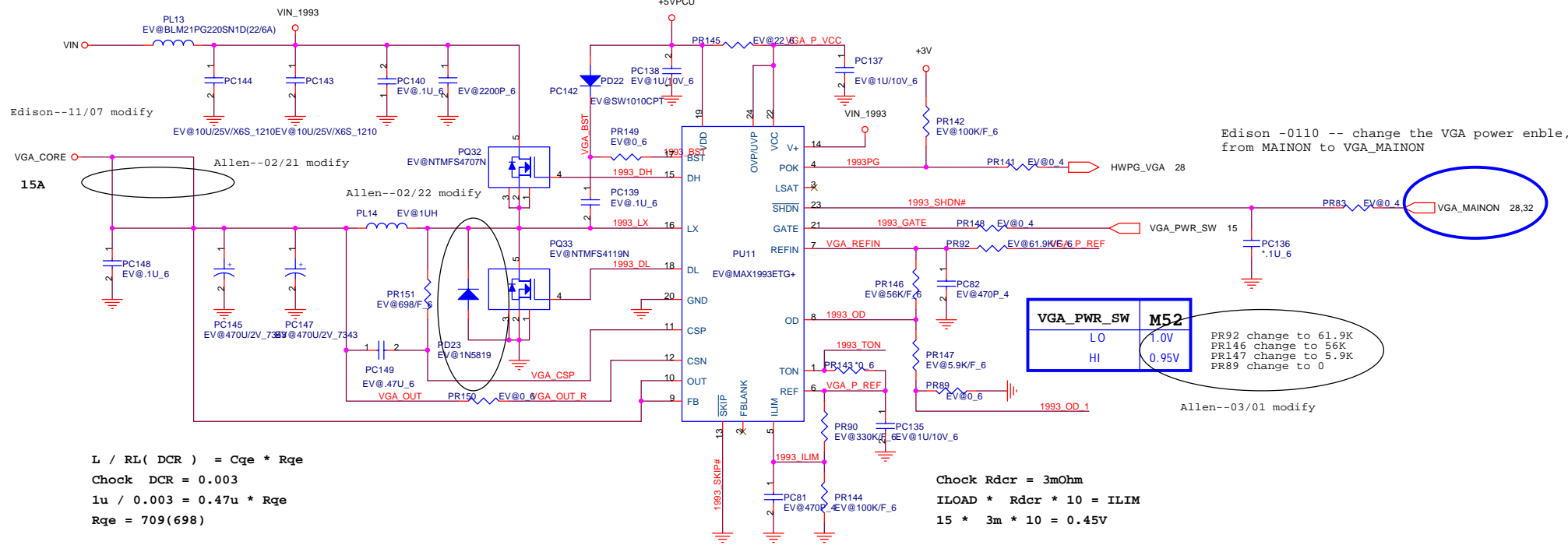


Switch

LED



PROJECT : ZB3  
Quanta Computer Inc.



# VGA CORE



Alan --11/17 Modify  
Reserve for VGA sequence

Allen --11/16 Modify

7.5A+3.5A for  
VCCP\_+1.05V

Allen--02/21 modify

$$VOUT = (1 + R2/R3) * 0.5$$

VCCP\_+1.05V

Allen--02/21 modify

3.5A

$$Vout1 = (1 + Rg/Rh) * 0.5$$

Edison --01/03 Modify



PROJECT : ZB3  
Quanta Computer Inc.

Size	Document Number	Rev
	DISCHAGE&+1.8V	1A
Date:	Monday, April 03, 2006	Sheet 32 of 37



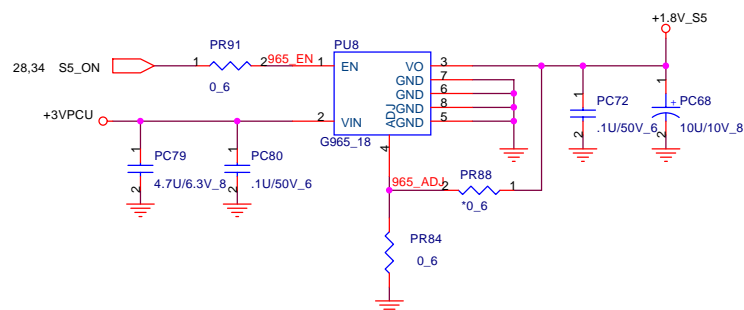
PC73 \*.1U/25V\_6  
5214\_OCDQ

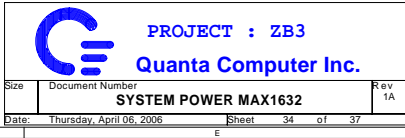
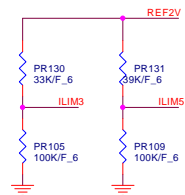
VIN\_NCP5214



Edison-11/10- Modify

Edison 0112 -- To change the PC182 from 0.1U to 10uF\_0805





# SYSTEM

## 3V & 5V

